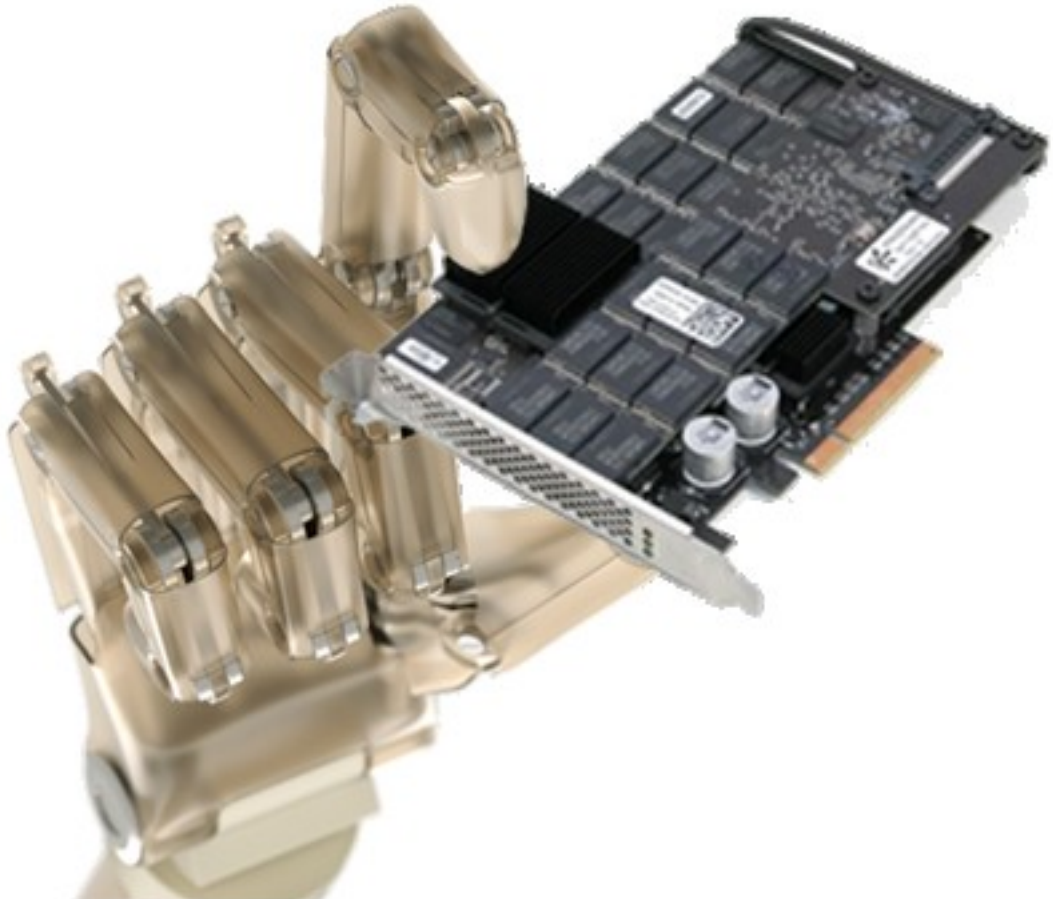
SNIA Solid State Storage Initiative
PCIe SSD Task Force Meeting No. 4

Monday 21 MAY 2012

WELCOME!

SNIA
Advancing storage & information technology

Meeting No. 4
Monday 21MAY2012
4:00 PM - 5:30 PM PST



Welcome to the SNIA
Solid State Storage Initiative

PCIe SSD Task Force

This is an Industry Task Force
d to investigate, discuss & educate
All things PCIe SSD

ship is Complimentary for (90) Days
ıe homepage at www.snia.org/forums/sssi/pcie

Task Force Participants

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Advancing storage & information technology

Concall Guidelines:

- Use your mute button
- ***Sign in webex w/ company name john smith (ABC Co.)***
- Be on time for roll call
- Un Mute when talking
- Use webex chat to ask questions

- Respond to Feedback Requests
- Email String Topic Discussions
- Email comments to reflector
  pciessd@snia.org
- Send Questions to
  pciechair@snia.org

(8) OPEN Meetings - Apr - Jul
SSSI Committee Aug - Dec 2012

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Topics	09APR12 Mtg No. 1	23APR12 Mtg No. 2	07MAY12 Mtg No. 3	21MAY12 Mtg No. 4	04JUN12 Mtg No. 5	18JUN12 Mtg No. 6	02JUL12 Mtg No. 7	16JUL12 Mtg No. 8	30JUL12 SSSI Committee
Kick-Off Mtg Issue Identification	X								
Standards		X							
Test Platforms		X							
Performance			X						
System Integration			X						
System Arch Form Factors				X					

Goals: Issue Identification & Committee 2012 Roadmap

Time: 4:00 – 4:05

(8) OPEN Meetings - Apr - Jul
SSSI Mtg & FMS Round Table

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Topics	04JUN12 Mtg No. 5	18JUN12 Mtg No. 6	02JUL12 Mtg No. 7	16JUL12 Mtg No. 8	30JUL12 SSSI Committee	20AUG12 Flash Memory Summit
Big Picture What's it all Mean	X					
Deployment Strategies Market Development		X				
Where do we go from here?			X			
Roadmap & Milestones 2012				X		
SSSI Committee Mtg					X	
SSSI Task Force F2F FMS Round Table **SNIA / SSSI Reception**						X

Tentative Topics for Meetings

Time: 4:00 – 4:05

AGENDA – 21 MAY 12

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I.	**Administrative**	
a.	Roll Call; Call Schedule	4:00 – 4:05
b.	Announcements; Survey for Mtg. No. 5 Discussion & Other	4:05 - 4:10
II.	**Business**	
1.	**Form Factors -**	
a.	**2.5" PCIe Form Factor - Janene Ellefson, Micron**	4:10 - 4:30
2.	**System Architecture**	
a.	**SCSI Express - Marty Czekalski, Seagate**	4:30 - 4:50
b.	**PCI SIG - Rick Eads, Aglient**	4:50 - 5:20
c.	**PCIe System & Form Factor Concerns - Rob Vezina, Aglient**	4:50 - 5:20
III.	**Wrap Up**	
a.	Discussion	5:20 – 5:30
b.	Close	

Time: 4:00 – 4:05

Attendance
1 of 4

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Company	No	09APR12	23APR12	07MAY12	21MAY12	04JUN12	18JUN12	02JUL12	16JUL12
Agilent	1	x	x	x	x				
Allion	2	x	x		x				
AMD	3	x	x						
Apacer	4								
BitSprings	5				x				
Cadence	6	x							
Calypso	7	x	x	x	x				
Cisco	8		x	x	x				
CLabs	9								
Corsair	10			x					
Coughlin Associates	11	x	x	x					
Dell	12	x							
eAsic	13	x			x				
EMC	14	x	x	x	x				
Enmotus	15	x			x				
eTron	16		x						
Fusion-io	17	x	x		x				
Greenliant	18		x	x	x				

Time: 4:00 – 4:05

Attendance
2 of 4

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Company	No	09APR12	23APR12	07MAY12	21MAY12	04JUN12	18JUN12	02JUL12	16JUL12
HDS	19	x		x	x				
HP	20	x	x	x	x				
HGST	21	x	x	x	x				
Huawei	22	x	x	x	x				
Hynix (SK Hynix)	23		x	x	x				
HyperIO	24	x	x	x					
IBM	25	x		x					
Intel	26	x	x	x	x				
Kingston	27								
Lecroy	28		x	x	x				
Lenovo	29	x		x					
LiteOnIT	30								
Link-A-Media	31								
Lotes	32								
LSI	33				x				
Lunastar	34	x	x	x	x				
Marvell	35		x		x				
Micron	36	x	x	x	x				
Microsoft	37	x	x	x					

Time: 4:00 – 4:05

Attendance
3 of 4

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Company	No	09APR12	23APR12	07MAY12	21MAY12	04JUN12	18JUN12	02JUL12	16JUL12
Molex	38	x	x	x	x				
Mushkin	39								
NetApp	40				x				
Objective Analysis	41	x			x				
OCZ	42	x							
Oracle	43	x	x	x					
PC Perspectives (Allyn M.)	44								
PLX Technology	45			x	x				
Phison	46	x	x	x	x				
Renesas	47	x	x	x	x				
Samsung	48	x	x	x	x				
Sandisk	49	x	x						
Seagate	50	x			x				
Semtech Snowbush IP	51								
Smart Storage	52		x	x	x				
SNIA	53	x	x	x	x				
STEC	54	x	x	x					

Time: 4:00 – 4:05

Attendance
4 of 4 - TOTAL (64) Companies

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Company	No	09APR12	23APR12	07MAY12	21MAY12	04JUN12	18JUN12	02JUL12	16JUL12
Taejin	55	x	x	x					
Tektronix	56								
TMS	57	x							
Toshiba	58		x	x	x				
Tyco Electronics	59	x	x						
Unigen	60	x	x	x					
Viking	61								
Virident	62	x	x	x	x				
WDC	63	x	x	x					
Paul Mitchell (Ind)	64								
		39	37	34	33				

Time: 4:00 – 4:05

Announcements - Eden Kim

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1. Announcements / Other
   a. Minutes Meeting No. 3 - next slide
   b. Task Force Charter / Structure - Standing Slides
   c. Announcements:
      1. Meeting No. 5 - General Discussion & Big Picture: What's it all mean
      2. Topics - See previous slide
      3. Task Force General Survey - feedback on first 4 meeting
      4. SSSI PCIe Round Tables:
         - Flash Memory Summit (closed)
         - Storage Developers Conference (contact pciechairs@snia.org)
      5. SNIA/SSSI Reception:

What: Tentative Reception : SSSI PCIe Committee - Roadmap 2012
Why: New Member Introduction; SSSI PCIe Committee Inauguration
Who: Invitation only : sponsored by SNIA and the SSSI
When: Monday 20AUG12 5:30 - 7:00 pm
Where: Santa Clara Convention Center 2d floor

Stay Tuned for More Information

Time: 4:05 – 4:10

Minutes Meeting No. 3
07MAY12

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1. **Attendance:**
   a. **(34) Companies present of (58)**
   b. **Presentations / Speakers - Calypso, HP, Virident, STEC**
2. **Administrative:**
   a. **Task Force Charter** - General Survey of PCIe SSD issues; Recommendations for SSSI Committee 2d half 2012
   b. **Task Force Structure -**
      1. **(8) Open Mtgs:** 09AP12, 23APR12, 07MAY12, 28MAY12, 04JUN12, 18JUN12, 02JUL12, 16JUL12
      2. **Meeting Topics:**
         General - up to (2) major discussions/meeting
         Presentations - Participants may present topics / slides during meetings - contact pciechair@snia.org
         Meeting No. 1 - Organizational; Survey Review; Overview of PCIe
         Meeting No. 2 - Standards: A Closer Look; PCIe Test Hardware Refresh
         Meeting No. 3 - PCIe Performance Test Issues; PCIe System Integration Issues
         Meeting No. 4 - System Architecture; Form Factors
         Meeting No. 5 - General Discussion / Q&A Submitted to reflector
         Meetings no. 6 - 8 - tbd
      3. **Links:** Email Reflector: pciessd@snia.org PCIe Task Force Homepage: www.snia.org/forums/sssi/pts
3. **PCIe Performance & SNIA SSS PTS - Easen Ho, Calypso**
4. **SNIA PTS Performance Saturation - Chuck Paridon, HP**
5. **System Integration H/W F/W - Hany Eskander, STEC**
6. **System Integration Device v System IOs - Tony Roug, Virident**
6. **Next Actions -**
   a. **Feedback on Meeting Topics - post to reflector**
   b. **Agenda / Topics - Meeting No. 4**

Close 5:30PM

Time: 4:00 – 4:10

Charter
Standing slide

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Task Force Charter: GENERAL SURVEY OF PCIE ISSUES

1. **Provide Guidance to Marketplace about PCIe SSDs**
    1. Educational Materials
    2. Best Practices Documents
    3. Industry Standards Work
2. **Coordinate w/ other Industry Organizations**
    1. Complement other groups
    2. Avoid Overlap
    3. Fill Voids
3. **Open Industry Forum to SSSI Committee**
    1. (90) Day Free Trial Membership
    2. SNIA SSSI Membership Required Aug 2012
    3. No IP/NDA - No Confidential Information may be discussed
    4. Identify Issues & Define Roadmap for Committee

Time: 4:05 – 4:20

Structure
Standing Slide

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Task Force Structure:

1. Webex Meetings - Every other Monday
    1. Starting Monday 09APR12 and every two weeks thereafter
    2. 4:00 PM - 5:30 PM PST
    3. (8) Open Calls prior to SNIA/SSSI Membership Requirement

2. Email Reflector - pciessd@snia.org
    1. Agenda, Minutes & Discussion via reflector until 30JUL12
    2. Post Meeting Survey's for feedback and agenda preparation
    3. Email reflector becomes SSSI member only starting 30JUL12

3. Target Objectives for (90) Day Public Forum Period
    1. Table of Standards Groups
    2. Recommendation on PCIe Hardware Test Platform Standard
    3. Identification of PCIe SSD Performance Issues
    4. Hosting of PCIe Round Table Panel
    5. Other Objectives defined by Task Force
    6. Identity Issues & Recommend SSSI PCIe Committee Roadmap for 2012

Time: 4:05 – 4:20

Links
Standing slide

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SSSI

- SSSI homepage — www.snia.org/forums/sssi
- Understanding SSD Performance Project — www.snia.org/forums/sssi/pts
- SSS Performance Test Specification (PTS) — www.snia.org/pts
- PTS Standard Report Format — www.snia.org/forums/sssi/pts
- SSSI Bright Talk Webcasts — www.snia.org/forums/sssi/knowledge/education
- SSSI White Papers — www.snia.org/forums/sssi/knowledge/education

PCIe Task Force

- PCIe SSD Task Force — www.snia.org/forums/sssi/pcie
- PCIe SSD Task Force reflector — pciessd@snia.org
- PCIe SSD Task Force questions — pciechair@snia.org

Time: 4:05 – 4:20

PCIe Form Factors - 2.5” PCIe SSD

Janene Ellefson, Micron

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PCIe 2.5” SSD

Janene Ellefson

Product Marketing Manager – eSSD

Micron Technology

Time: 4:10 - 4:30

PCIe Discussion Topic

Janene Ellefson, Micron Technology

- PCIe SSD traditional Form Factors
  - HHHL Card
  - FHHL Card
- Advantages
  - High Performance
  - High Density
- Disadvantages
  - No Hot Plug
  - Exposed components
  - Not easily accessible

Time: 4:10 – 4:30

PCIe Discussion Topic

Janene Ellefson, Micron Technology

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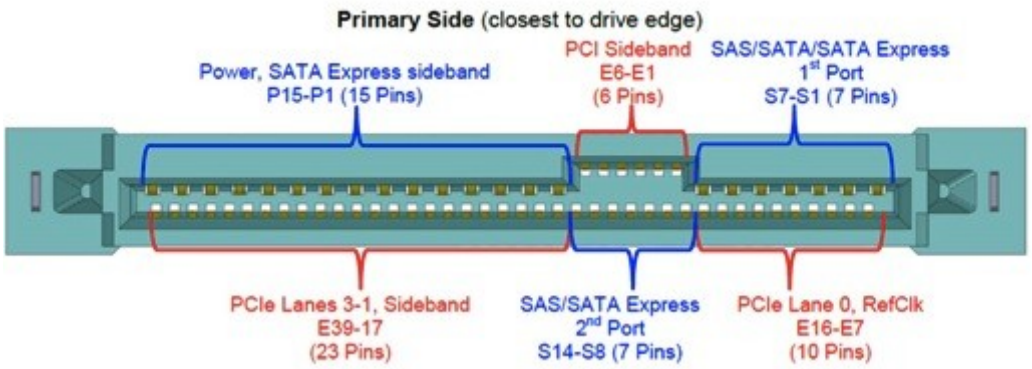
- **SSD Small Form Factor Working Group**
  - http://www.ssdformfactor.org/
- **Key Objective: Provide Scalability, Accessibility, Compatibility, Hot Plug**
- **2.5" PCIe SSD**
  - **Shared backplane**
  - **External access**
  - **Common form factor**
  - **Combo connector** (SFF-8639)



Time: 4:10 – 4:30

PCIe Discussion Topic

Janene Ellefson, Micron Technology

- **Benefits**
  - **PCIe performance**
  - **Hot Plug**
  - **Scalability**
  - **Serviceability**
  - **Lower TCO**
  - **Rugged Form Factor**

Time: 4:10 – 4:30

PCIe Form Factors - 2.5” PCIe SSD

Janene Ellefson, Miron

- **Discussion / Questions & Answers**

Time: 4:20 - 4:35

SCSI Trade Assoc.: SCSI Express

Marty Czekalski, Seagate

1. Item

Time: 4:30 - 4:50

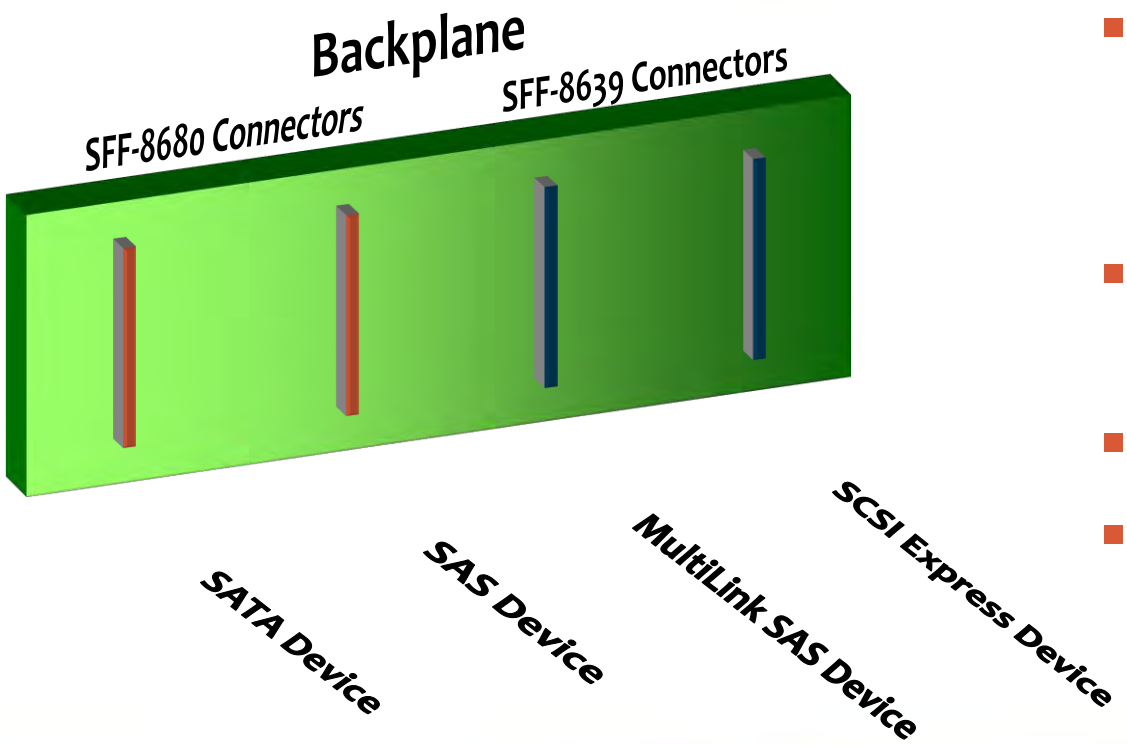
Advancements in PCIe Storage

SCSI Express

STA
SCSI Trade Association

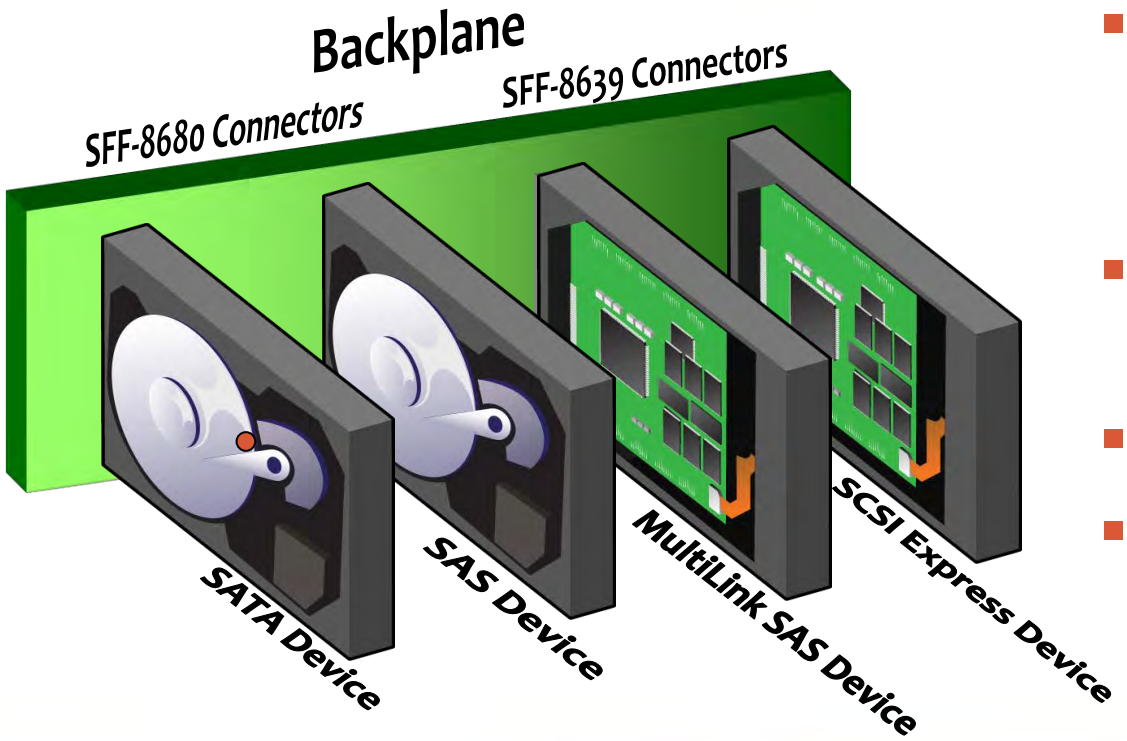
Proven SCSI protocol combined with PCIe creates industry standard path to PCIe-based storage

Express Bay



- Enhances PCIe storage experience within the enterprise
- Multi-protocol connector (SFF-8639)
- Serviceable bay
- Power provisioned for SSD-class performance (up to 25W)

Express Bay

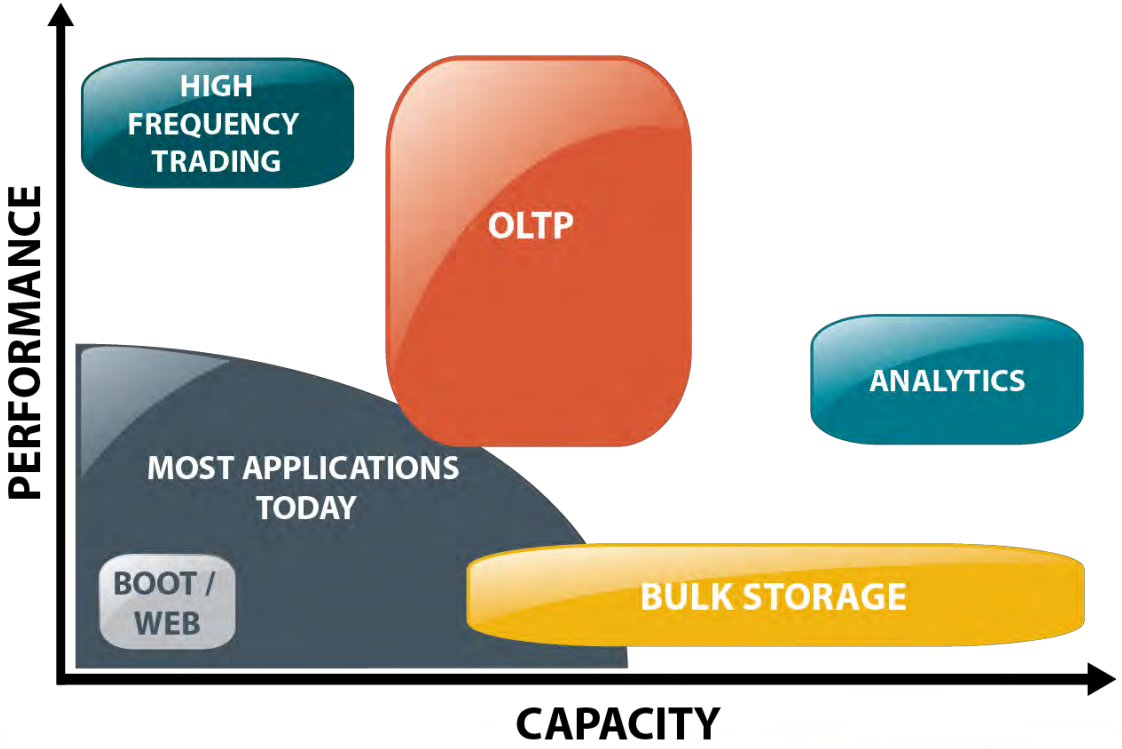


- Enhances PCIe storage experience within the enterprise
- Multi-protocol connector (SFF-8639)
- Serviceable bay
- Power provisioned for SSD-class performance (up to 25W)

Benefits of SCSI Express

- Brings enterprise-class SCSI storage to PCIe
- Enables tiered/caching environments
- Preserves SCSI management, feature set, and tools
- Extends storage investments, leveraged to PCIe
- Provides co-existence with SAS

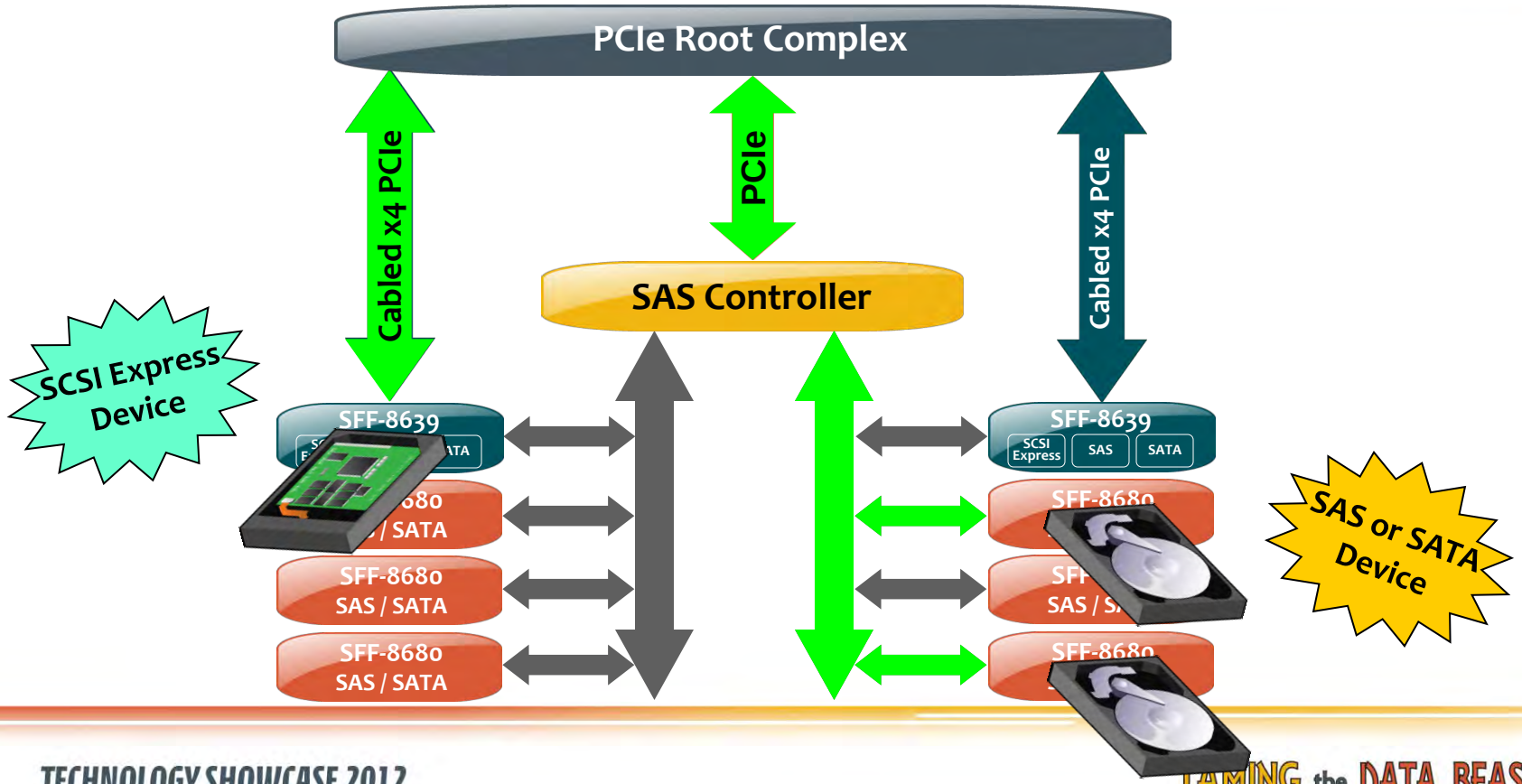
SCSI Express Use Cases



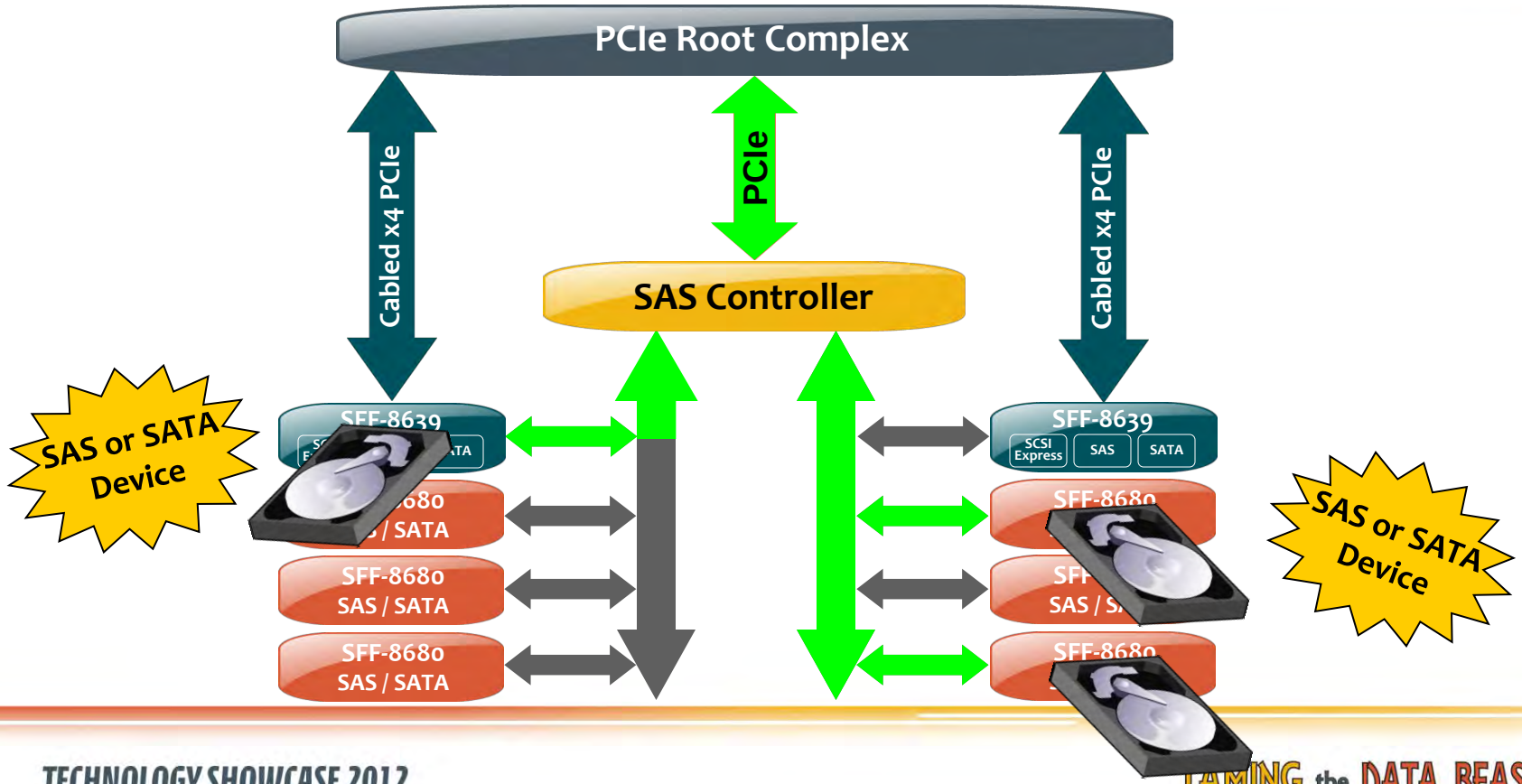
Ideal for:

- Caching
- Financial trading
- Database
- Virtualization
- Online transactions
- Web hosting

What's Being Demonstrated?



What's Being Demonstrated?



SCSI Express:

The Smart Path to PCIe Storage

Ron Noblett

HP - Vice President, Infrastructure & Storage
Industry-standard Servers & Software, Hyperscale

Barry Luck

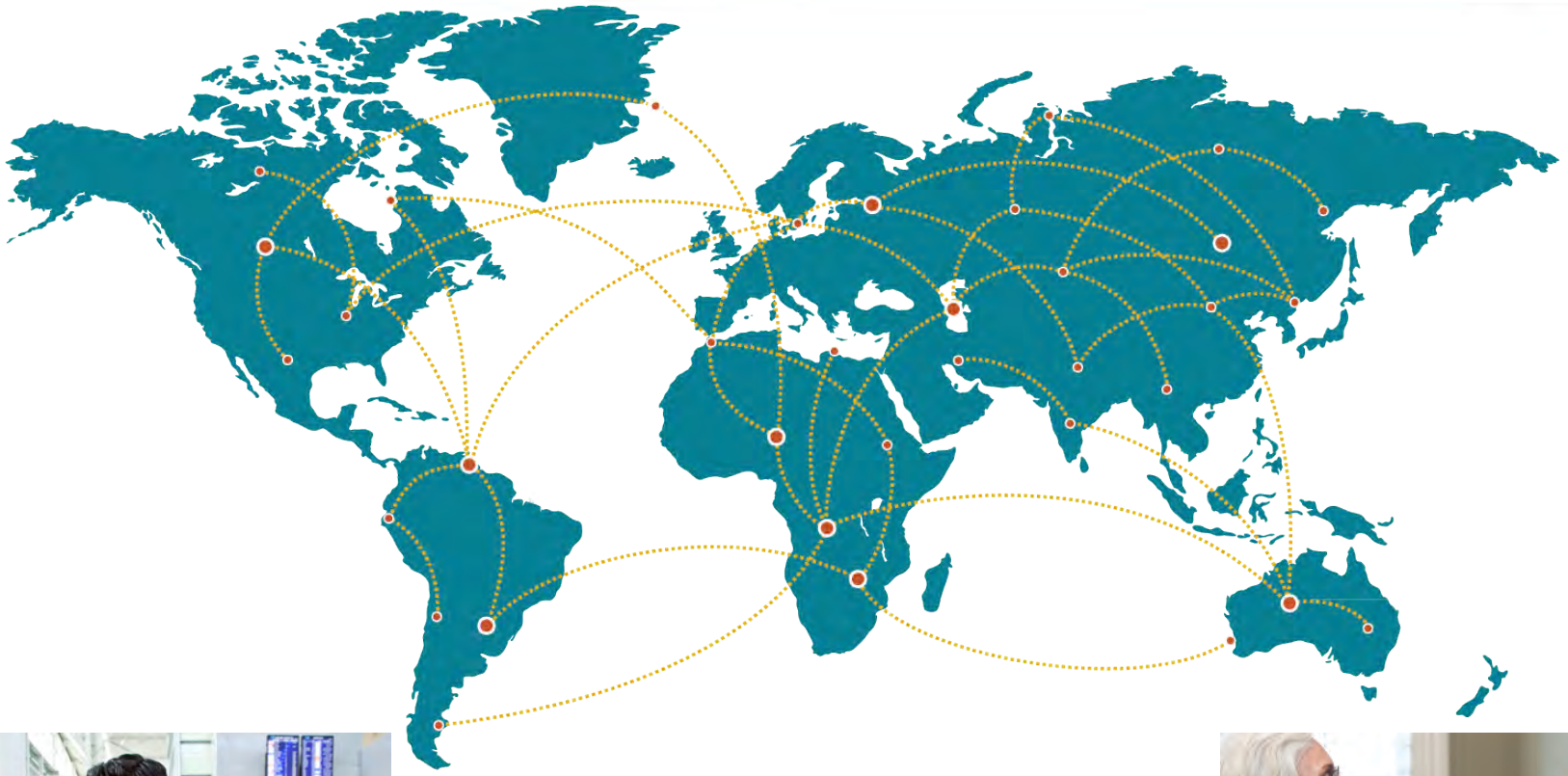
IBM - Director, Next Generation
Platforms, Ecosystems

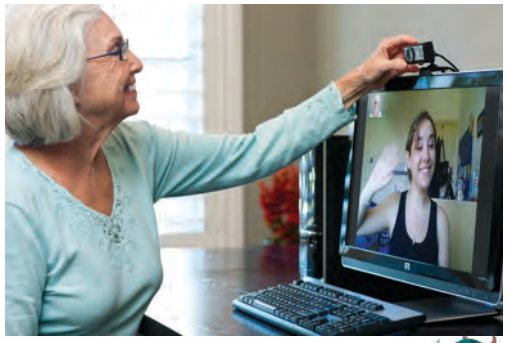
Keeping up in a cloud-enabled world

SCSI Trade Association

Respond to increasing demands for data

The world is changing





The best of the best prevail

SCSI Trade Association

SCSI EXPRESS

PCI EXPRESS® + SCSI

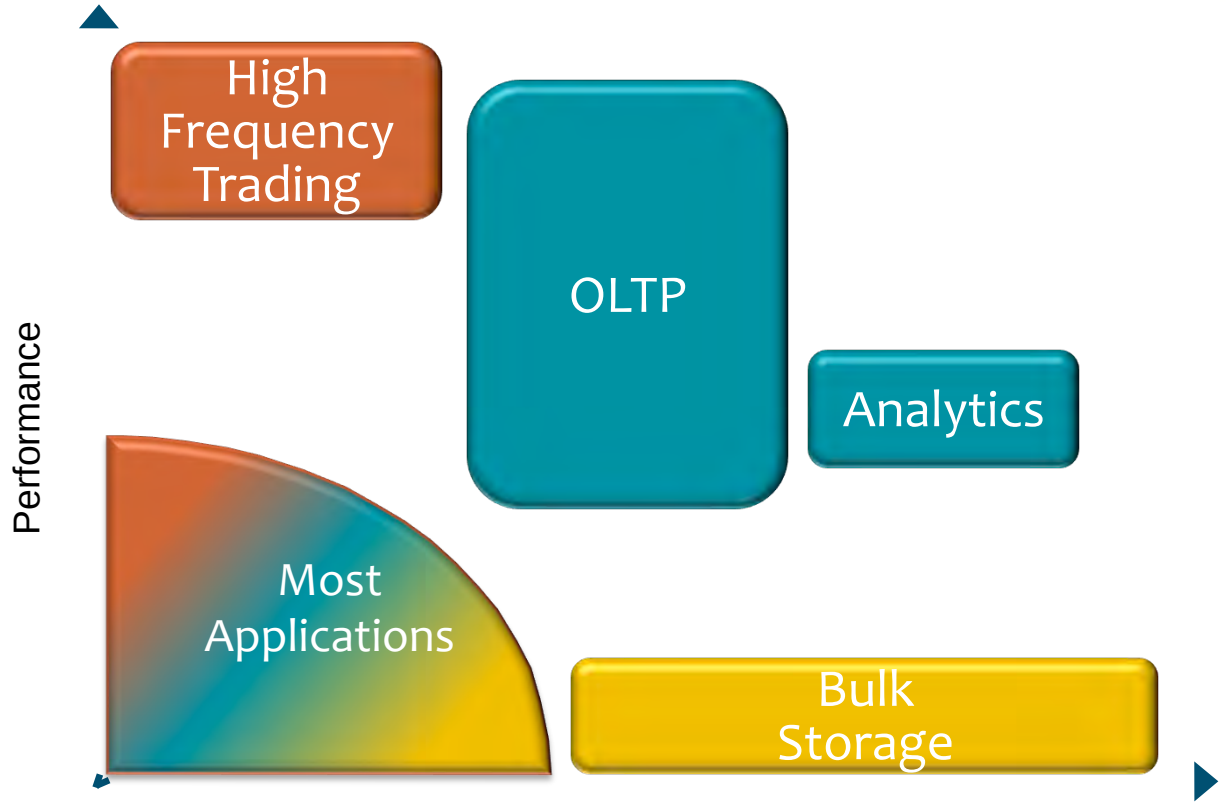
What is SCSI Express?

SCSI Trade Association

SCSI EXPRESS

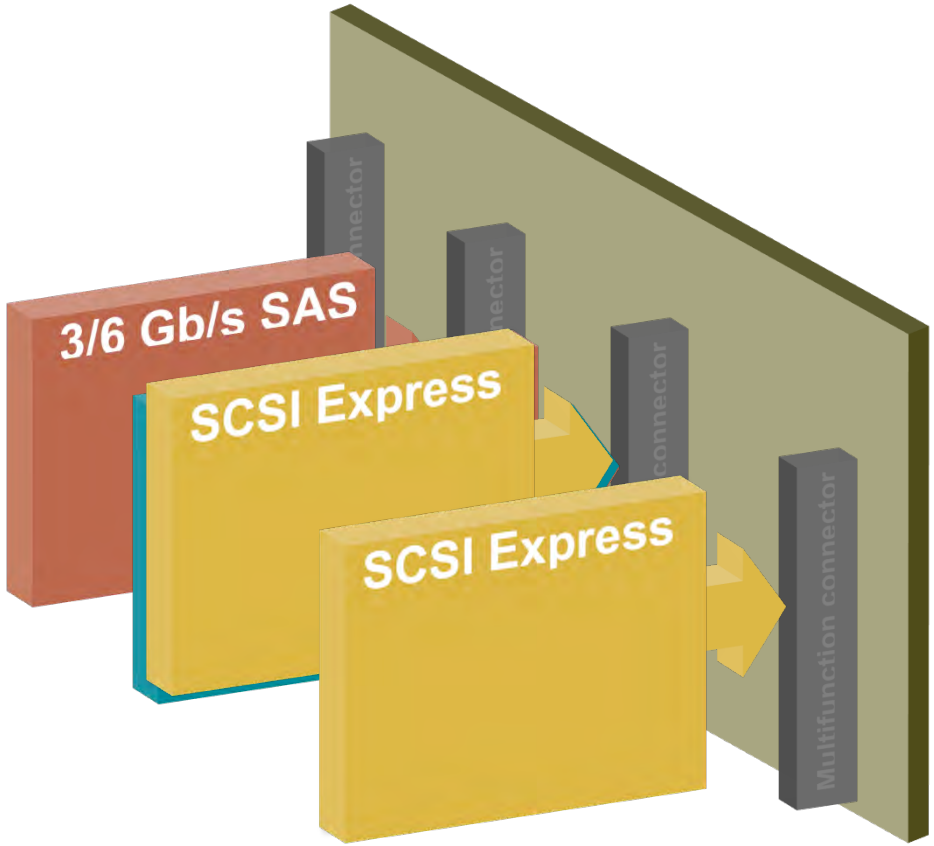
MISSION	TARGET	METHOD
Accelerate and streamline data storage	Enterprise server and storage systems	SCSI command optimizations
Unlock the full potential of solid state devices	Solutions balancing SAS and SCSI Express	PCI Express enhancements

Unlimited opportunity for SCSI



- Solid State
- HDD + Solid State
- HDD

The Future is bright with Express Bay



SCSI Express, 3/6 Gb/s SAS, & 12Gb/s SAS with a single multifunction connector

Thank you.

Visit our demo stations to see what T10 and STA are doing to respond to today's business challenges.

SCSI Trade Assoc.: SCSI Express

Marty Czekalski, Seagate

- **Discussion / Questions & Answers**

Time: 4:30 - 4:50

System Architecture - PCI SIG

Rick Eads & Rob Vezina, Agilent

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- **PCI-SIG**

Bio:
Rick Eads

Rick Eads is a senior product manager with expertise in technical/industrial marketing of test and measurement tools and electronic design automation software to leaders in the computer, semi-conductor, wired and wireless communications, storage and aerospace industries worldwide. Rick works on precision product definition and synthesis of breakthrough solutions that address new and emerging needs for both software and hardware products. He provides technical leadership in driving standards within industry organizations for PCI Express, ExpressCard, FB-DIMM (FBD), DDR, HyperTransport, ExpressCard, SATA, and InfiniBand. He has worked in marketing test and measurement products covering oscilloscopes, Logic Analyzers, microprocessor emulation solutions, ASIC emulation tools, EDA tools.

Rick earned a M.B.A. from the University of Colorado with an emphasis on finance and marketing, and he graduated with a BSEE from Brigham Young University with an emphasis on digital design and computer architecture. He holds three patents and has published numerous papers and technical articles.

Time: 4:50 - 5:20

PCIe Discussion Topic
Name, Company

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- PCI SIG Structure
  1. Best Practices (A perspective from 1 of the 9 active Board of Directors)
- Specification Development Process
  1. How to write a specification
     - Silicon Specification (defining the operation of ICs)
     - Form Factor Specification (integration of IC's into endpoint and other systems)
     - Test Specification Development (how to test and validate the above specifications)
- Specification Approval Process (Integrated Board of Director approval/milestones)
  1. Autonomous Group organization and working conventions
  2. Cross Functional Working Group review process
  3. Member review process
- PCI SIG Funded Compliance Program (delegation of activity across Working Groups)
  1. PHY Layer Compliance
  2. Link Layer/Protocol Compliance
  3. Demonstrated Interoperability
  4. Public Integrator List & Logo Program
- Contracting/outsourcing Logistics/Management of all above activities to external contracting firms

Time: 4:25 – 4:40

Agilent Standards and Applications Program

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- Our solutions are driven and supported by Agilent experts involved in international standards committees:
  - Joint Electronic Devices Engineering Council (JEDEC)
  - PCI Special Interest Group (PCI-SIG®)
  - Video Electronics Standards Association (VESA)
  - Serial ATA International Organization (SATA-IO)
  - Serial Attached SCSI (T10)
  - USB-Implementers Forum (USB-IF)
  - Mobile Industry Processor Interface (MIPI) Alliance
  - Optical Communications
  - And many others
- We're active in standards meetings, workshops, plugfests, and seminars
- We get involved so you benefit with the right solutions when you need them

JEDEC
PCI EXPRESS
SERIAL ATA
HDMI HIGH-DEFINITION MULTIMEDIA INTERFACE
USB
mipi mobile industry processor interface

Agilent Digital Standards Program Leadership

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Memory Perry Keller	USB Jim Choate	Computer Rick Eads	Storage Min Jie Chong	Consumer Electronics Brian Fetz
Board of Directors JEDEC	PHY C&I Chair WiMedia Technical Lead USB-IF Compliance Committee Primary Representative WiMedia Compliance Review Board	Board of Directors PCI-SIG	Contributor Serial ATA Working Group	Board of Directors VESA

Compliance Testing

- **Ethernet** compliance application
- **PCI EXPRESS** compliance application
- **HDMI** compliance application
- **SAS** compliance application
- **DisplayPort** compliance application
- **MIPI D-PHY** compliance application
- **10GBASE-T** Automated Test Application
- **WiMedia** Wrapper Compliance Test Application
- **SATA 6Gb/s** Compliance
- **USB 3.0** Compliance Software
- User Defined Application

The Agilent Digital Standards Team directs the company's engagement in the top high tech standards organizations

PCI-SIG PCI Express Standards Organization

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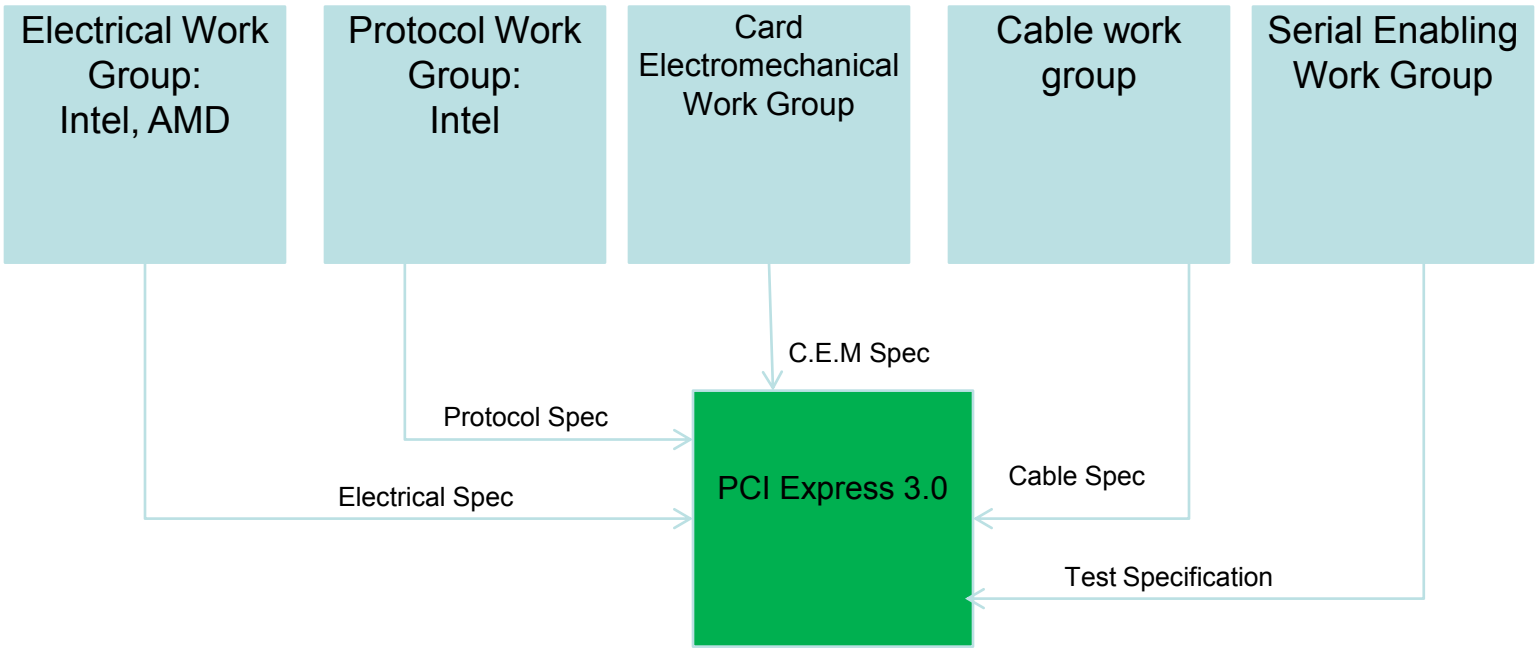
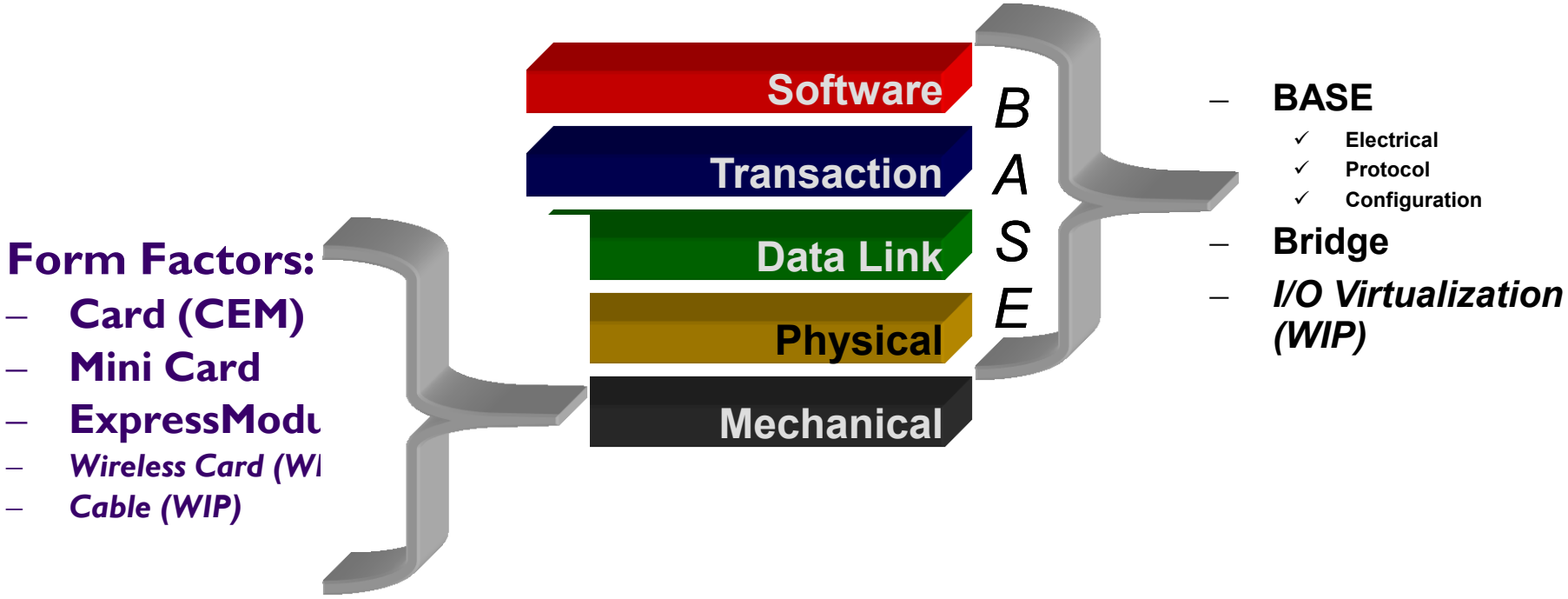
PCI Express Board of Directors
Agilent, Intel, IBM, LSI Logic, Dell, HP, Sun Microsystems, nVidia, AMD

PCI-SIG Executive Director: Reen Presnel, VTM

Legal: Tim Haslach



PCIe Architecture Specifications



- CEM includes some electrical (for that form factor)
- Designed to match to applications
- Member developed (volunteer leadership in work groups)

PCI-SIG Compliance Process

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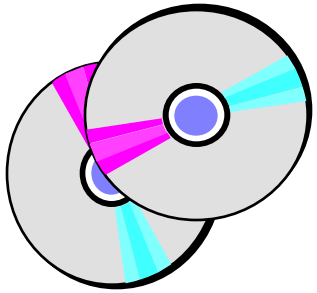

Test Tools
And Procedures

Workshops

C&I Test Specs

Interpret

- •Checklists
- •Assertions

Define

Test Criteria

- •Test Definitions

Test H/W & S/W

Validates

Test Criteria

- •Compliance
- •Interoperability

Clear Test Output

Maps

Directly to Test Spec

Predictable path to design compliance

Compliance Workshop Overview

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- Workshops are usually announced 2 months in advance
- System and card vendors register for the compliance workshops
- Systems are set up in suites
- PCI-SIG systems are set up
- Test schedule is developed
  - Indicates when cards are to be tested in the systems
  - Each card & system vendor receives a schedule for their product
  - Test forms are used to record the results of the testing

PCIe 3.0 Compliance Test Overview

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- **Physical layer**
  - 3.0 CLB and CBB fixtures
  - New Sigtest
    - Reference CTLE+DFE
    - Test Channel Embedding
  - New Clock Tool
    - Provides clock phase jitter test to 3.0 base specification
  - PLL Bandwidth
- **Configuration Space**
  - Updated PCIeCV for new fields and capabilities
- **Link & Transaction layer**
  - Run existing 2.0 tests at 8.0GT/s for 3.0 8GT/s capable devices
  - New tests covering link equalization and other new features
- **Platform Configuration**
  - PCIe 1.x PTC BIOS tests
  - Run existing tests at 8GT/s

Test Specs released at .7 revision level

Interoperability Testing

- Opportunity for vendors at compliance workshop to test with each other
- Goal is to demonstrate interoperability between products
- 80% passing rate required for eligibility for PCI-SIG integrator's list
- Demonstrate that the link can train and operate at 5GT/s if both devices support 5GT/s
  - For 3.0 8GT/s devices, demonstrate link at 8GT/s

PCI Express® 3.0 – Agilent Total Solution

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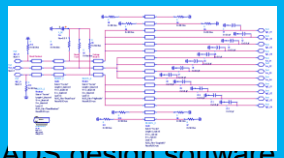
Physical layer – interconnect design



ADS design software

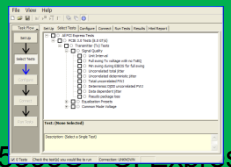
86100D DCA-J/TDR

N5230C PNA-L VNA

Industry's lowest scope noise floor/sensitivity and trigger jitter

Physical layer-transmitter test

9000 cope



N5 ss electrical compliance software

E m Waveform Transformation Software

DCA ultra low jitter

Physical layer-receiver test

J-BERT N4903B –complete receiver tolerance

N4880A Clock Multiplier and N4916B 4-tap de-emphasis signal converter

N5990A automated compliance and device characterization test software

Automated compliance software – accurate, efficient and consistent

Data link/transaction layer

- U4301A Protocol Analyzer
- U4305A Exerciser
- Multiple probes with ESP technology

X1 through x16 Analysis and Exerciser support, with industry's only ESP probing technology

Electrical Validation of Transmitters

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PCIe Validation for PC devices

Add-in Card Testing

PCI-SIG AIC Test Fixture (CBB3)

Motherboard Testing

PCI-SIG System Test Fixture (CLB3 x1x16)

PCI Express* 3.0 Add-in Card Test Fixture

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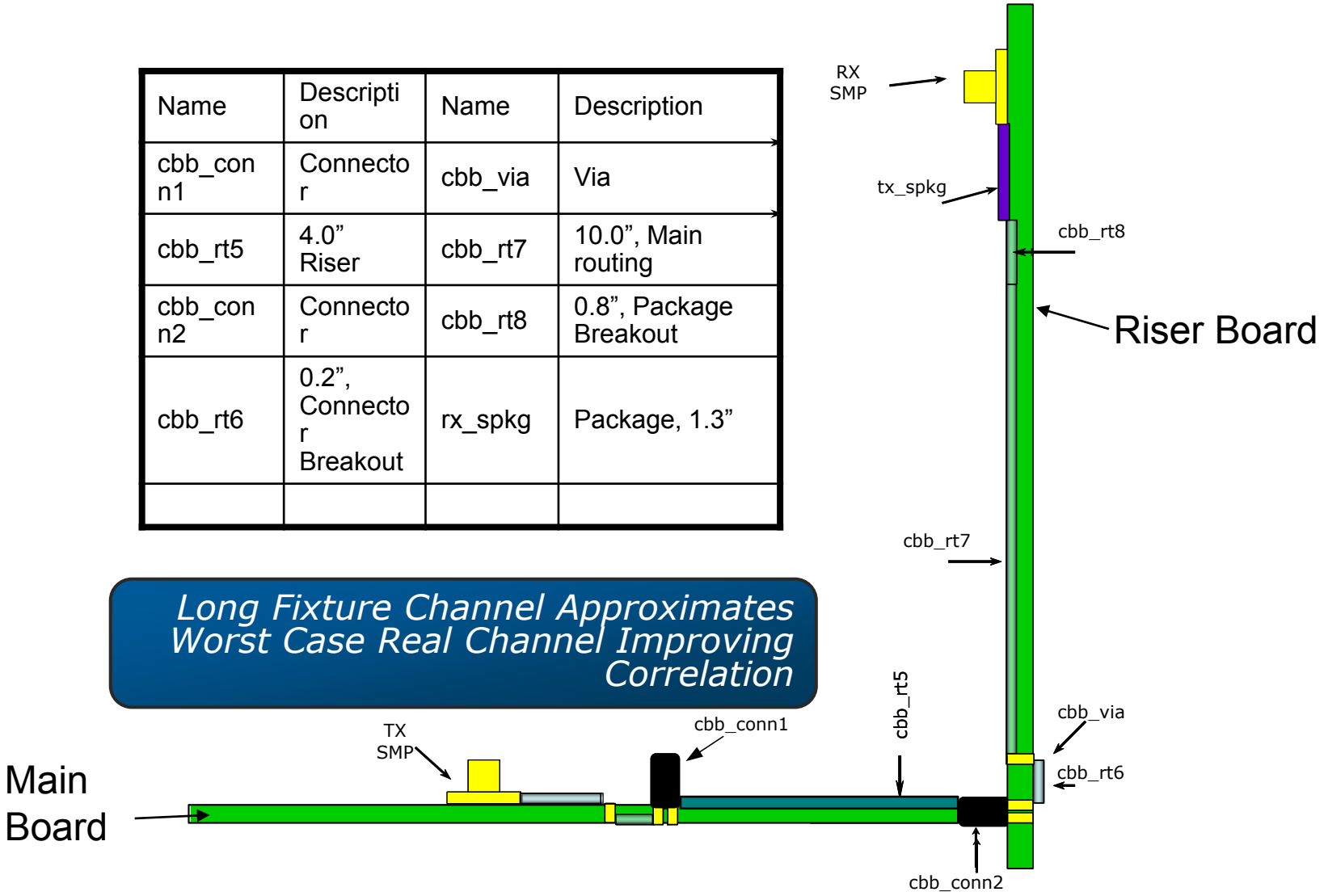
Name	Description	Name	Description
cbb_conn1	Connector	cbb_via	Via
cbb_rt5	4.0” Riser	cbb_rt7	10.0”, Main routing
cbb_conn2	Connector	cbb_rt8	0.8”, Package Breakout
cbb_rt6	0.2”, Connector Breakout	rx_spkg	Package, 1.3”

Long Fixture Channel Approximates Worst Case Real Channel Improving Correlation



PCI Express CEM Add-in-Card Compliance

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CBB3

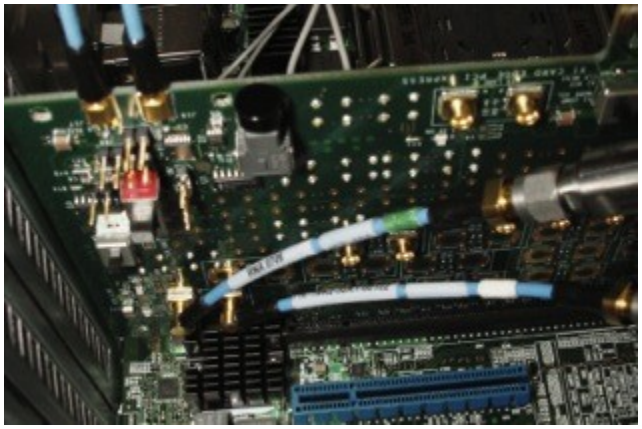
Low Loss SMA-SMA Cables

SMA/SMP Adapters

PCI Express CEM Root Complex Compliance

SMA/SMP Adapter

Ref Clock



CBB3

Low Loss SMA-SMA Cables

Compliance Toggle

Electrical Validation of Transmitters

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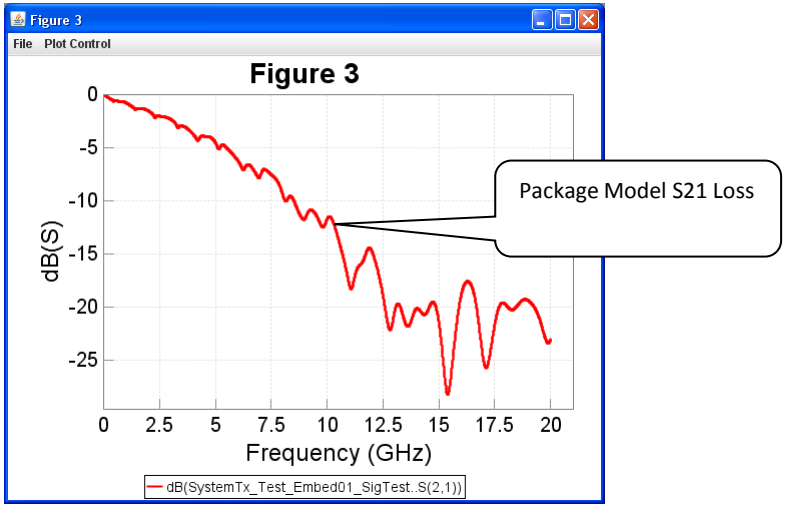
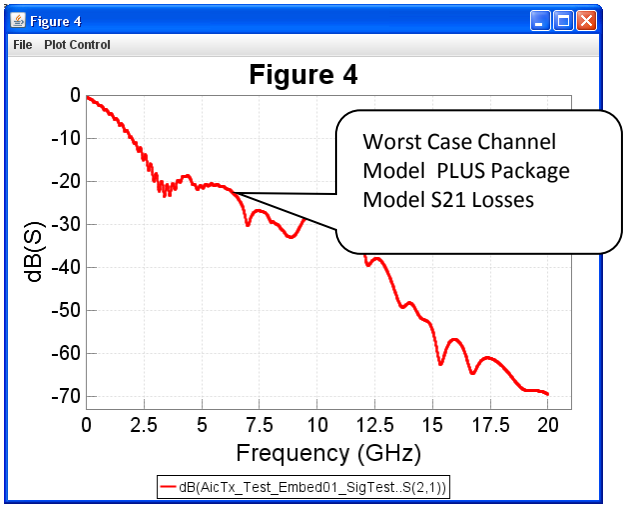
CEM Testing Procedures

Motherboard Testing



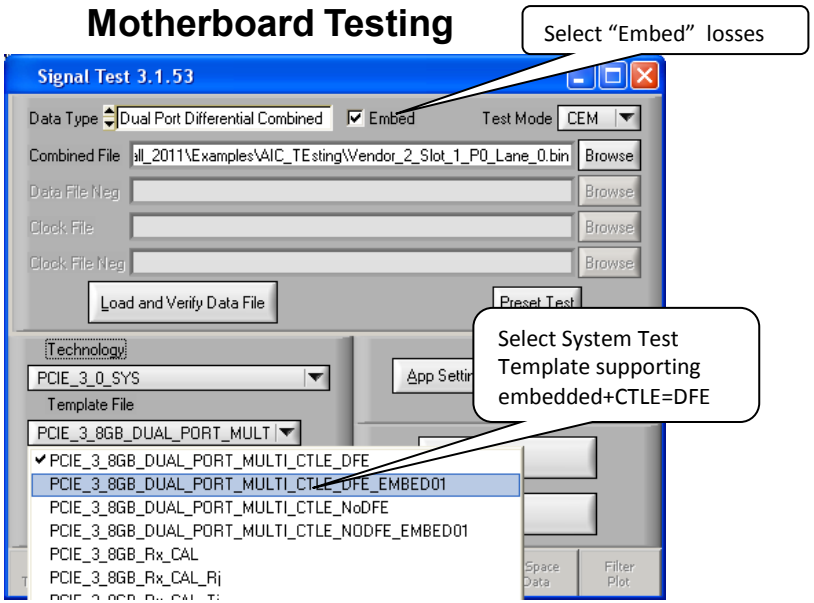
Add-in Card Testing



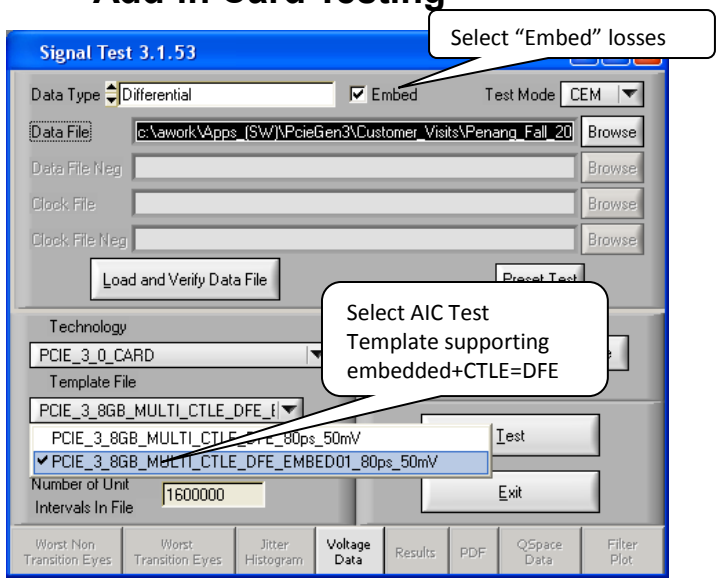
- Embed loss using Agilent InfiniiSim
  - Embed loss using Sigtest Embed Template selection

Testing Transmitters with PCIe Validation for PC devices

Motherboard Testing



Add-in Card Testing



Testing Transmitters with SigTest

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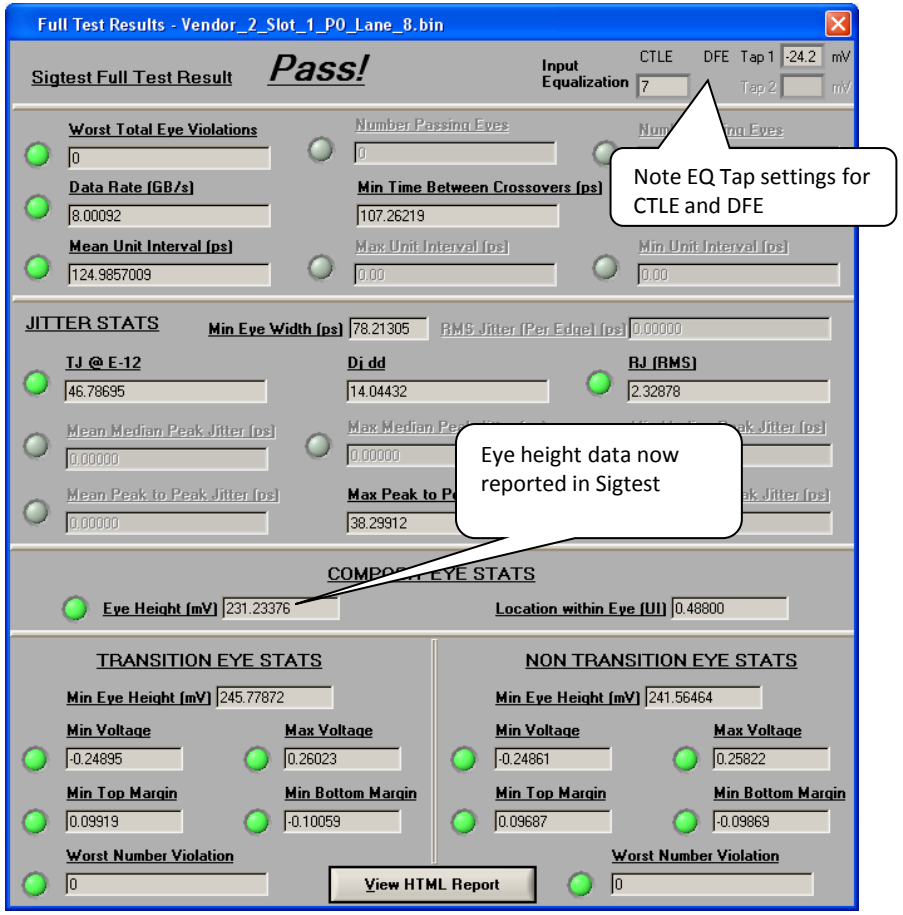
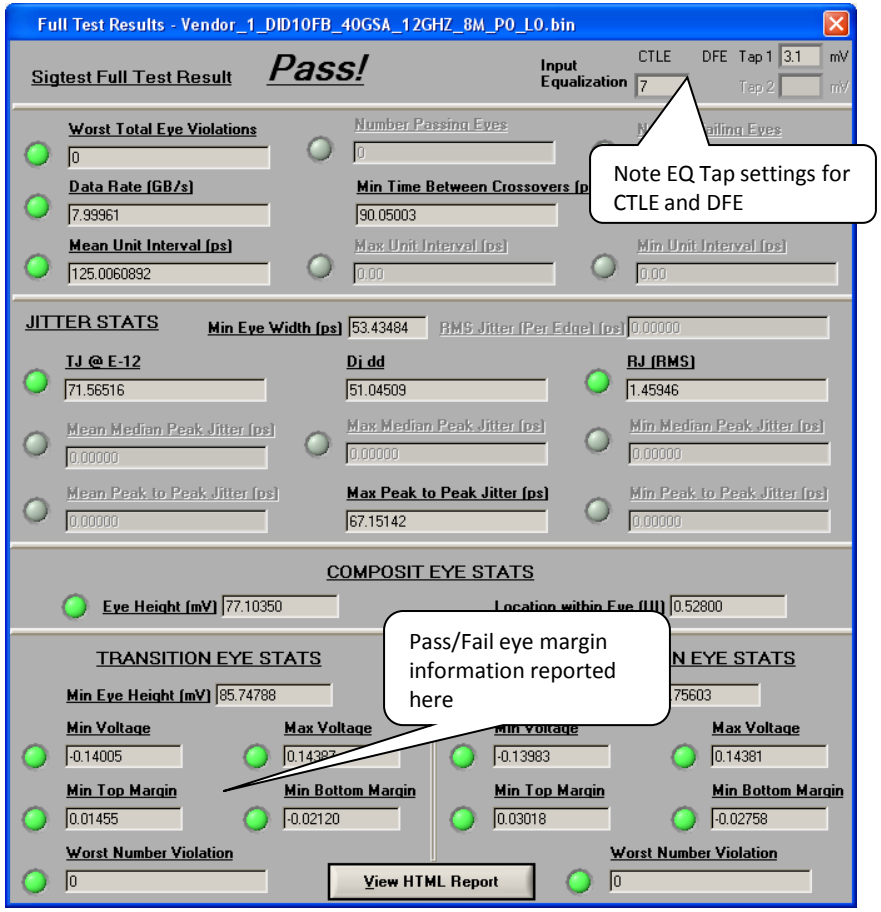
PCIe Validation for PC devices

Motherboard Testing



Add-in Card Testing



Testing Transmitters with SigTest

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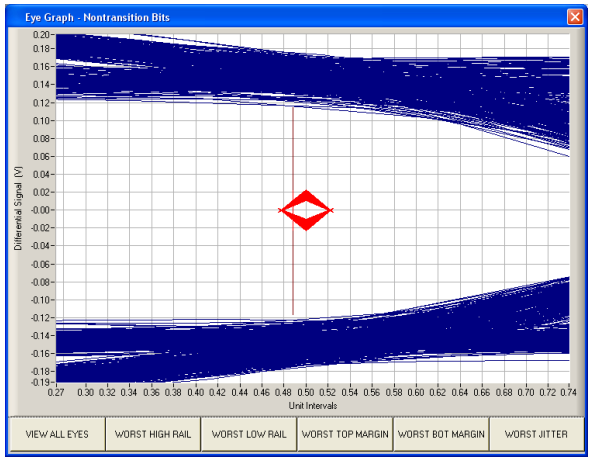
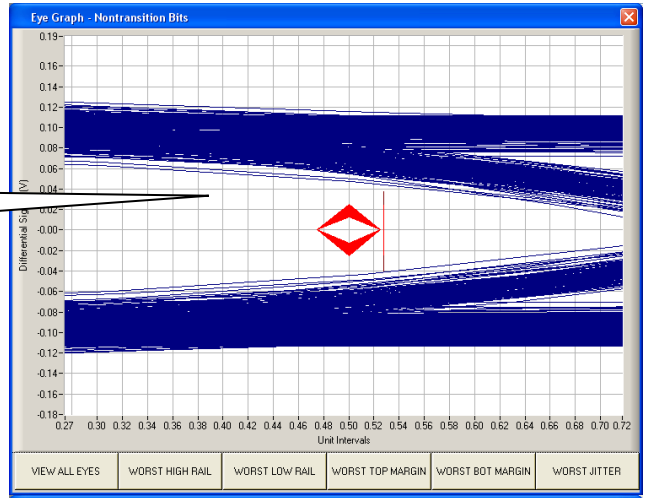
PCIe Validation for PC devices

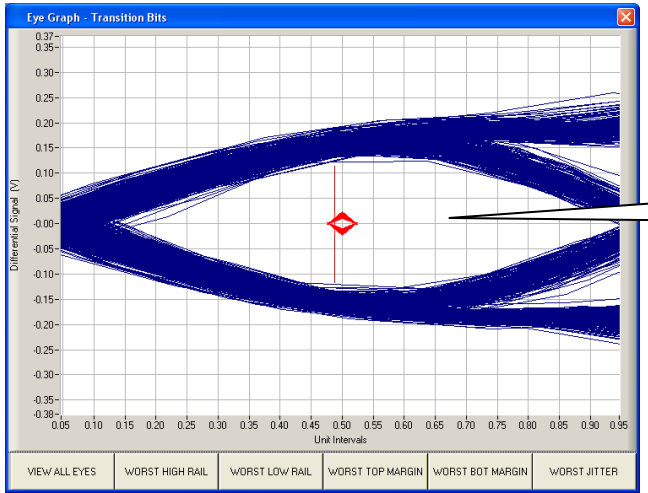
Motherboard Testing



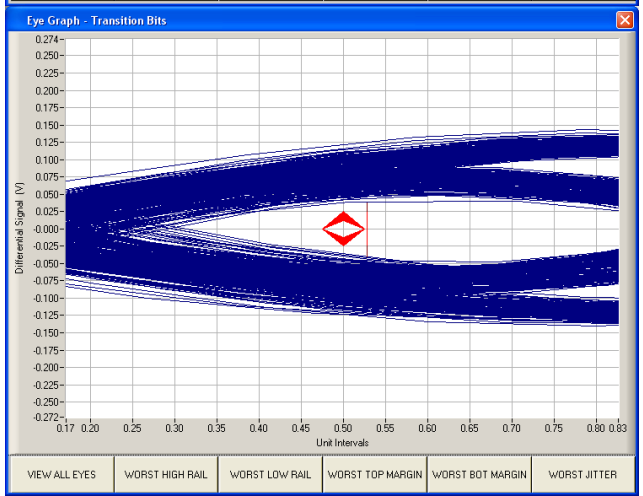
Add-in Card Testing



Non Transition Eye post embedding+CTLE+DFE



Transition Bit Eye post embedding+CTLE+DFE



Agilent N5393C TX Test Application

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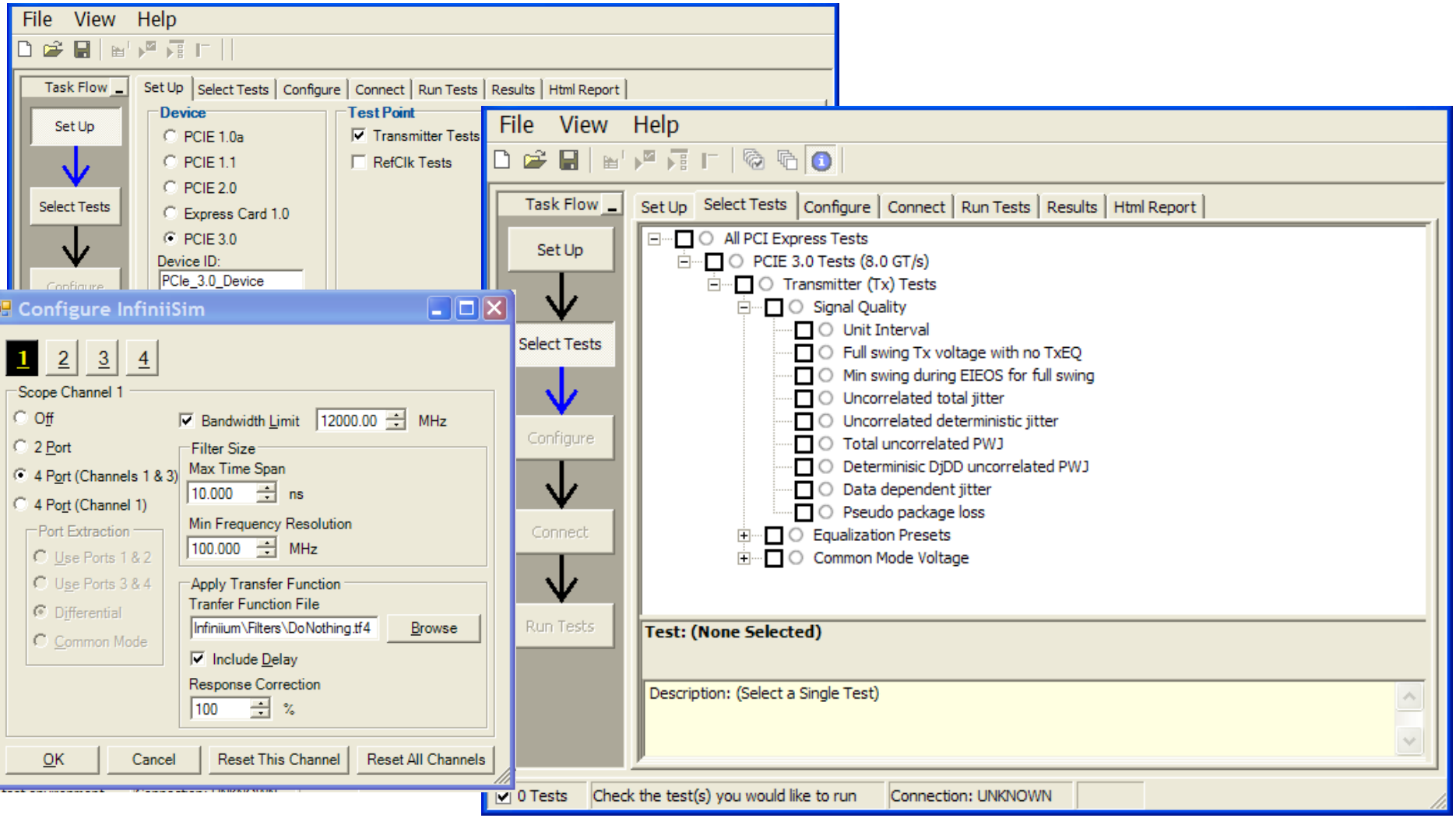

N5393C TX Test Application

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Agilent Technologies

PCI Express Test Report

Overall Results: 12 of 26 Tests Failed

Test Configuration Details	
Device Description	
Device ID:	Device 1
Test Session Details	
Infiniium SW Version	03.01.0002
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY47481312
Application SW Version	0.99.9018
Last Test Date	12/9/2010 2:25:17 PM

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	Tx, Unit interval (PCIE 3.0, 8.0 GT/s)	125.0010ps	48.7 %	124.9600ps <= VALUE <= 125.0400ps
✓	0	1	Tx, Full swing Tx voltage with no TxEQ (PCIE 3.0, 8.0 GT/s)	980.7mV	45.2 %	800.0mV <= VALUE <= 1.2000V
✓	0	1	Tx, Min swing during EIEOS for full swing (PCIE 3.0, 8.0 GT/s)	957.3mV	282.9 %	VALUE >= 250.0mV
✓	0	1	Tx, Uncorrelated total jitter (PCIE 3.0, 8.0 GT/s)	7.821ps	75.0 %	VALUE <= 31.250ps
✓	0	1	Tx, Uncorrelated deterministic jitter (PCIE 3.0, 8.0 GT/s)	1.009ps	91.6 %	VALUE <= 12.000ps
✓	0	1	Tx, Total uncorrelated PWJ (PCIE 3.0, 8.0 GT/s)	9.267ps	61.4 %	VALUE <= 24.000ps
✓	0	1	Tx, Deterministic DjDD uncorrelated PWJ (PCIE 3.0, 8.0 GT/s)	1.891ps	81.1 %	VALUE <= 10.000ps
✓	0	1	Tx, Data dependent jitter (PCIE 3.0, 8.0 GT/s)	9.943ps	44.8 %	VALUE <= 18.000ps
✓	0	1	Tx, Pseudo package loss (PCIE 3.0, 8.0 GT/s)	425mdB	114.2 %	VALUE >= -3.000dB

N5393C TX Test Application

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Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

De-emphasis Result for each Gen3 Preset

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	Tx, Full swing Tx voltage with no TxEQ (PCIE 3.0, 8.0 GT/s)	9[illegible].1mV	39.8 %	800.0m V <= VALUE <= 1.3000 V
✓	0	1	Tx, De-emphasis Preset #0 (PCIE 3.0, 8.0 GT/s)	-6.1397dB	45.3 %	-7.5000 dB <= VALUE <= -4.5000 dB
✓	0	1	Tx, De-emphasis Preset #1 (PCIE 3.0, 8.0 GT/s)	-3.6954dB	40	
✓	0	1	Tx, De-emphasis Preset #2 (PCIE 3.0, 8.0 GT/s)	-4.2832dB	46	
✓	0	1	Tx, De-emphasis Preset #3 (PCIE 3.0, 8.0 GT/s)	-2.2623dB	38	
✓	0	1	Tx, Preshoot Preset #5 (PCIE 3.0, 8.0 GT/s)	1.7665dB	43	
✓	0	1	Tx, Preshoot Preset #6 (PCIE 3.0, 8.0 GT/s)	2.2379dB	36	
✓	0	1	Tx, De-emphasis Preset #7 (PCIE 3.0, 8.0 GT/s)	-6.0455dB	48	
✓	0	1	Tx, Preshoot Preset #7 (PCIE 3.0, 8.0 GT/s)	3.5287dB	48	
✓	0	1	Tx, De-emphasis Preset #8 (PCIE 3.0, 8.0 GT/s)	-3.2598dB	38	
✓	0	1	Tx, Preshoot Preset #8 (PCIE 3.0, 8.0 GT/s)	3.2355dB	36	
✓	0	1	Tx, Preshoot Preset #9 (PCIE 3.0, 8.0 GT/s)	3.6573dB	42	
✓	0	1	Tx, De-emphasis Preset #10 (PCIE 3.0, 8.0 GT/s)	-7.7604dB	29	

✓ Tx, Preshoot Preset #7 (PCIE 3.0, 8.0 GT/s)

Reference: PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16

Test Summary: Pass | Test Description: | The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.

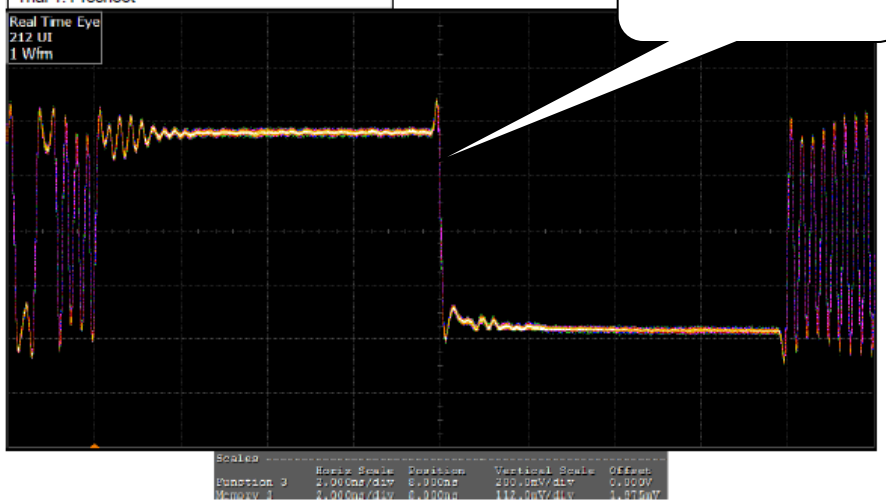
Test Limits: [2.5000 dB to 4.5000 dB] | **Preshoot** 3.5287dB

Result Details

Vb P7 406.450mV | **Vb P2** 610.160mV | **Lane Number** Lane 0 | **Connection**

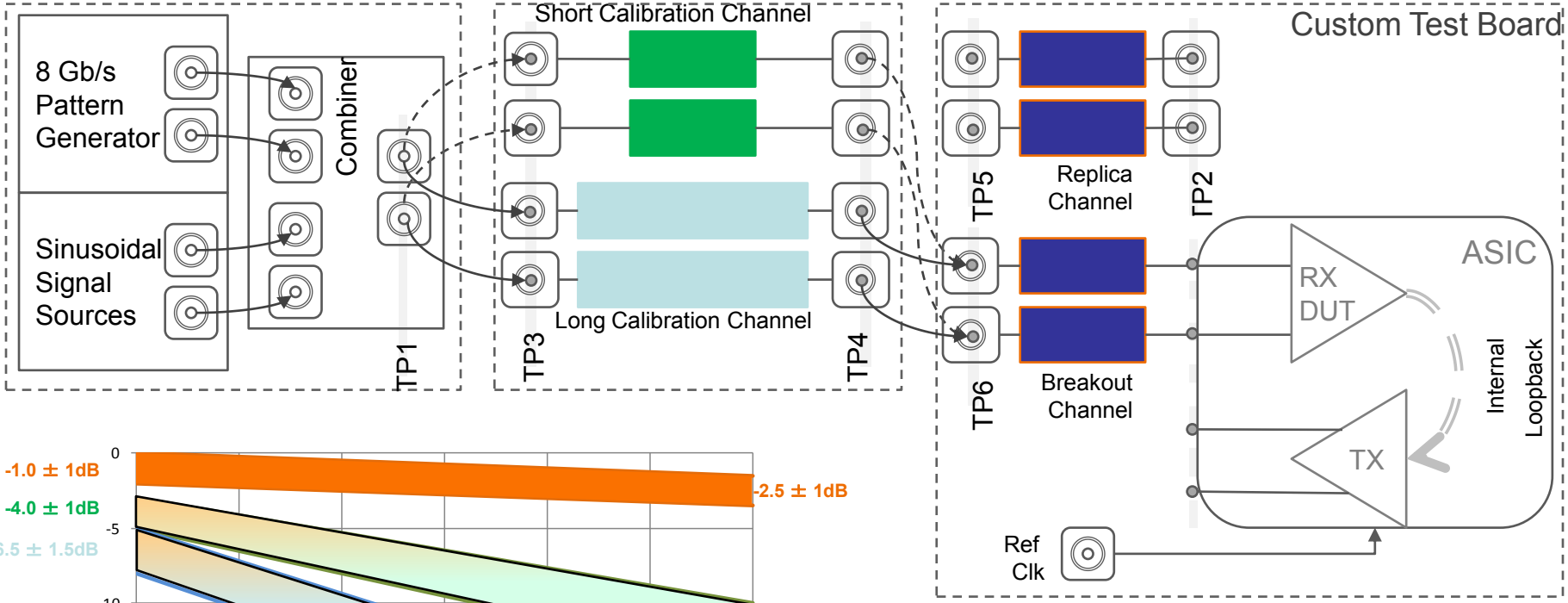
Trial 1

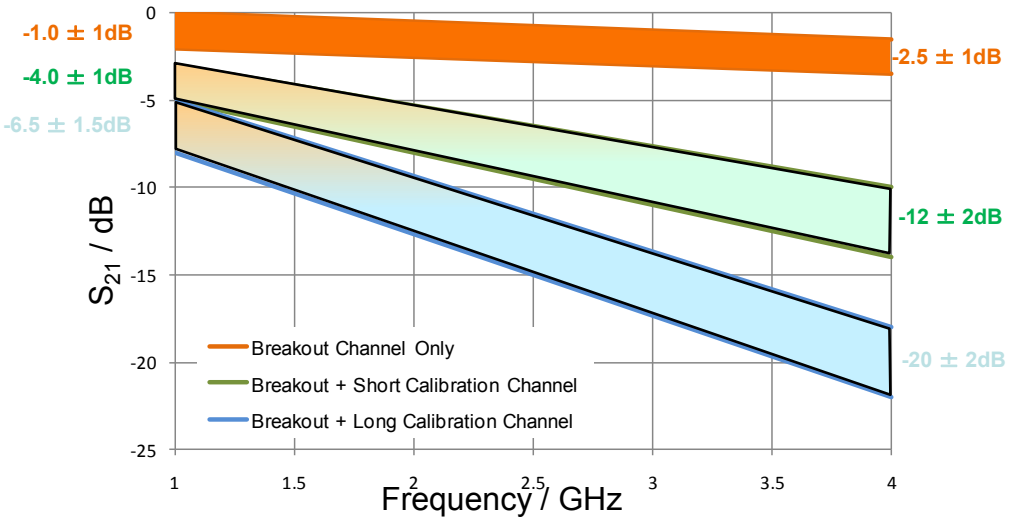
Trial 1: Preshoot



Report Detail includes waveform captures useful for debug.

RX Test-set-up acc. to PCIe3 Base Spec.





Emulation of different target applications is achieved with different channel lengths:
Three test cases have been defined :

- Break-out channel only (2.5dB @ 4GHz)
- Break-out + short cal chan. (9.5dB @ 4GHz)
- Break-out + long cal chan. (17.5dB @ 4GHz)

System Architecture - PCI SIG

Rick Eads & Rob Vezina, Agilent

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- **Discussion / Questions & Answers**

Time: 4:50 - 5:20

PCIe System & Form Factor Concerns

Rob Vezina, Agilent Technologies

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1. PCI Express 3.0 System Configuration
2. PCIe 3.0 Trace Capture Architecture

Summary Bullets:

- *All Tier1 PCIe 3.0 Tool Vendors provide similar system configurations*
- *SATA Express and SCSI over PCIe (SOP) have unique undefined PHY layer considerations which are not covered in this presentation*

Time: 4:50 - 5:20

System Configuration
Typical Root Complex (CPU) to DUT (MSI GFX card)

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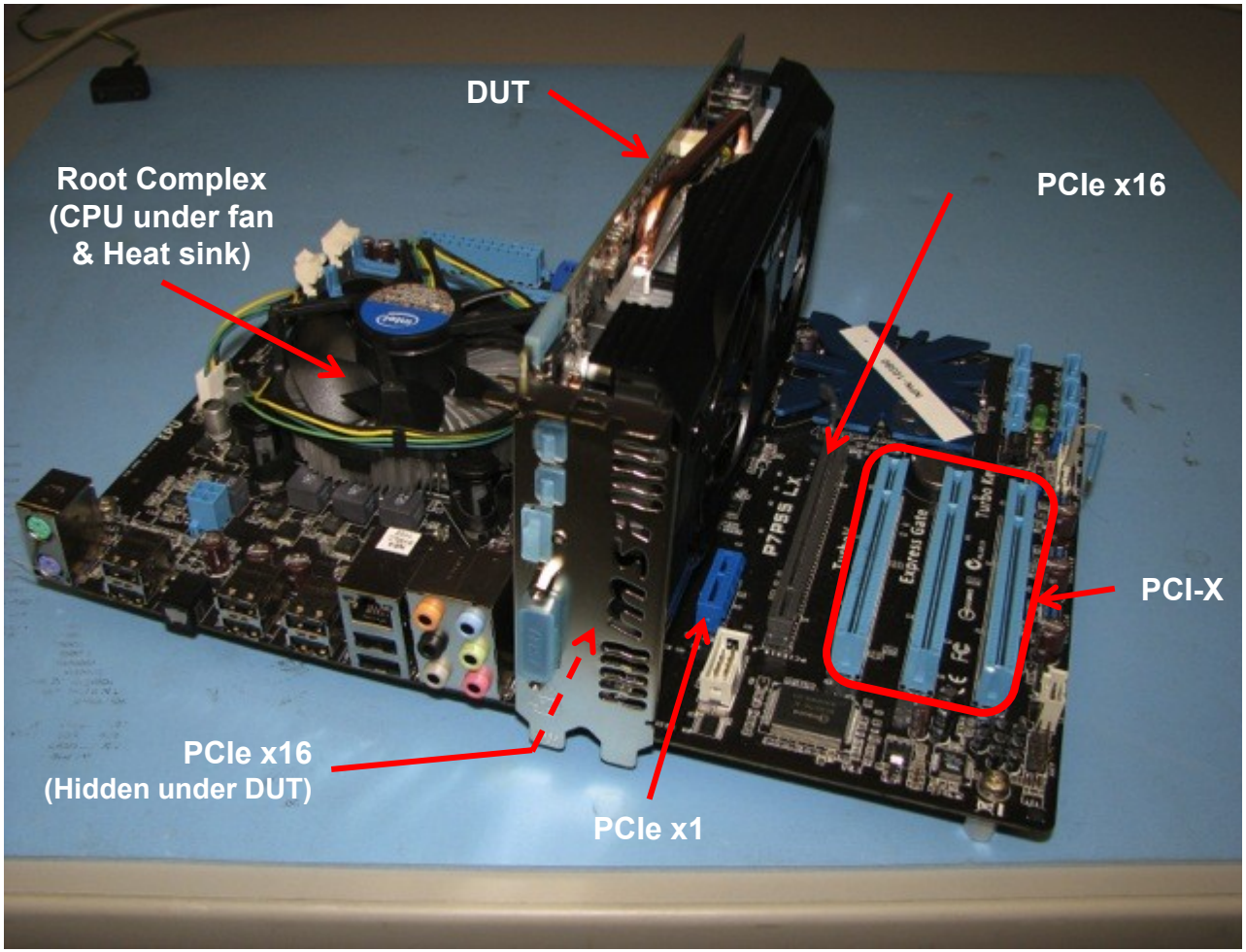

- The CPU on the motherboard is referred to as the Root Complex (RC)
- The MSI GFX card is the Device Under test (DUT)
  - The MSI GFX DUT is a **PCIe 3.0, x16 lane width, bidirectional device** therefore requires a 32 channel (32 PCIe 3.0 links) connection to the RC
  - The PCB MB x16 connector has 32 links to the RC therefore can support x16, bidirectional DUT
- 32 PCIe 3.0 links directly connect the RC to the DUT (via x16 connector)

Time: 4:50 - 5:20

System Configuration
Trace Capture Between Root Complex (RC) and DUT

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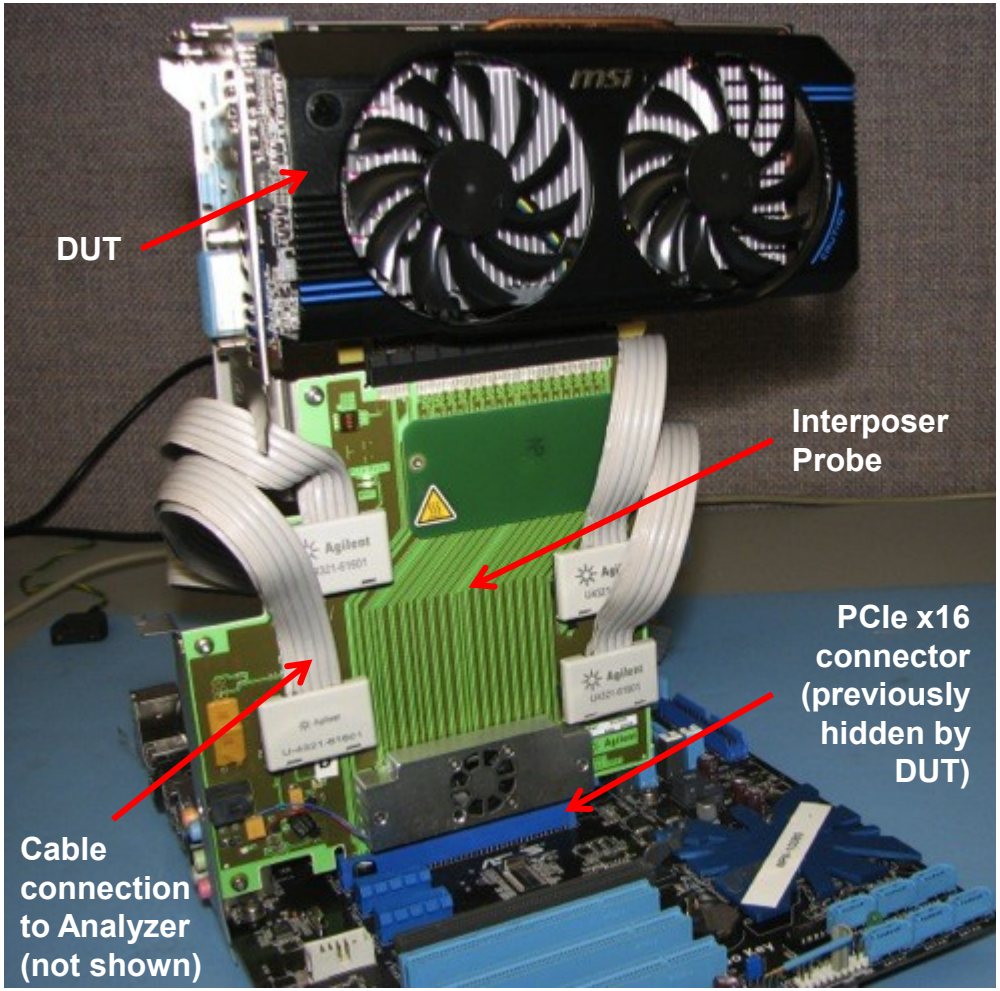

- The Interposer probe is installed between the RC and DUT. Protocol packets (or traffic) are passed between the RC and the DUT through the probe
- The 4 cables attached to the Interposer probe connect to the Protocol Analyzer module (not shown)
  - Each Interposer probe cable supports up to 8 PCIe 3.0 links. Therefore the 4 cables provide 32 links **or** 16 links in each direction **or** x16 bidirectional lanes
- Bidirectional means protocol packets are passed back and forth between the RC and the DUT simultaneously
- Downstream packets travel from the RC to the DUT. Upstream packets travel from the DUT to the RC
- PCIe 3.0 specification supports 8, 5, and 2.5 GHz link speed (1 GHz = 1 GT/s).
- A PCIe 3.0 lane net throughput is 16 GT/s (8 GT/s upstream and 8 GT/s downstream)

Time: 4:50 - 5:20

System Configuration

PCIe3 Root Complex (CPU) Emulation using an Exerciser and Backplane

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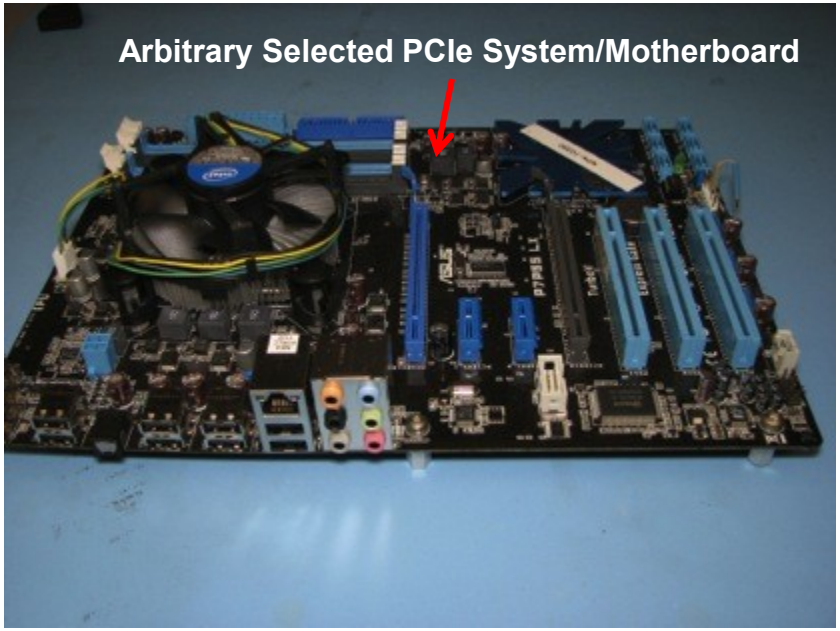

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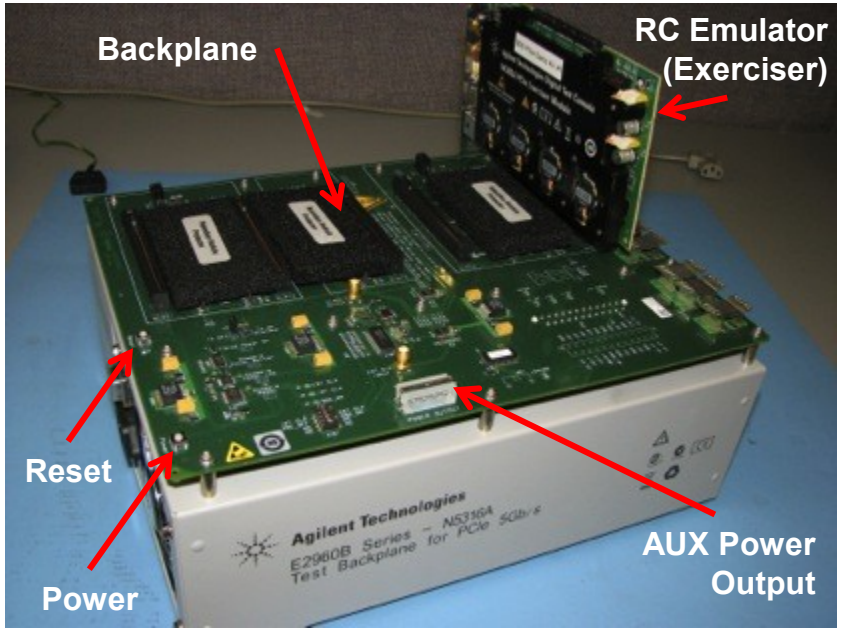

Why use RC Emulation

- No availability of PCIe 3.0 motherboard or CPU
- Full PCIe 3.0 Protocol control of the DUT
- DUT functional isolation from the Root Complex
- Internal or external reference clock source options
- Isolate crosstalk and jitter present on the motherboard
- Second source option for RC to validate DUT issue root cause

Time: 4:50 - 5:20

Benefits of the Backplane

- Allow testing of an end node without access to RC system
- Provides power and clock to the DUT (via Test Fixture)
  - Power, Reset + AUX power for DUT if required
  - Clock generator with/without SSC* selectable
  - Input for external reference clock
- All link widths supported – x1, x2, x4, x8, and x16
- Connectors: Two (2) independent x16 PCIe connector pairs (Link 1&3) & one x16 PCIe connector with loop back (Link 2)

*SSC – Spread Spectrum Clock (data rate modulation)

System Configuration
RC Emulator to DUT via Backplane Connection

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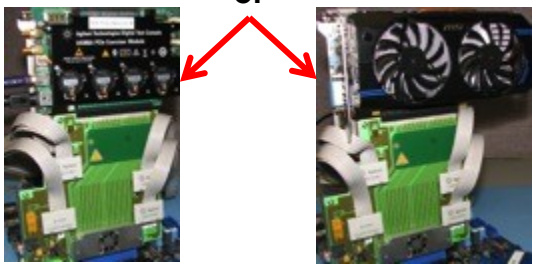
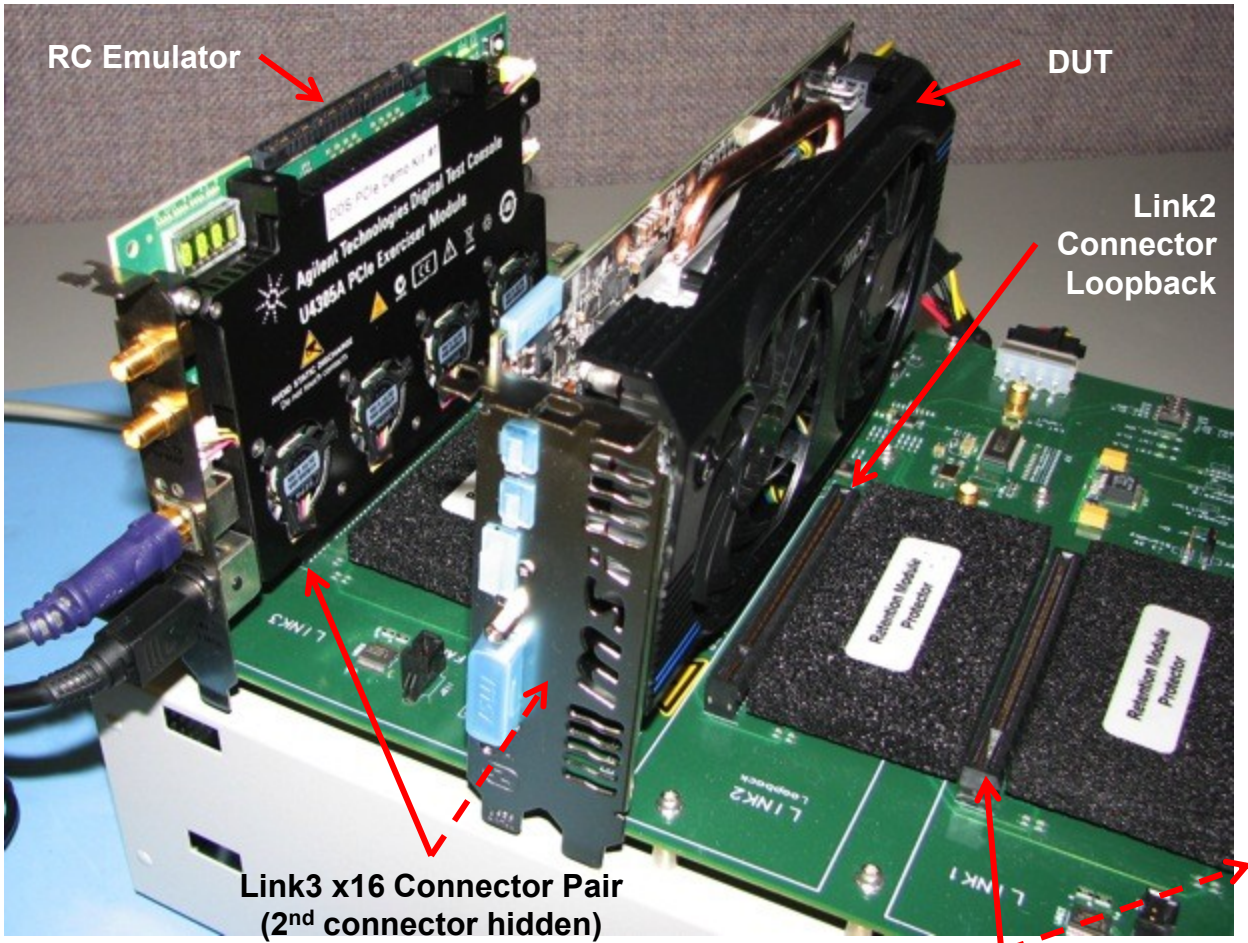
- Using the Link3 x16 connector pair, the Exerciser is configured as a RC and is linked to the DUT
- This configuration also happens to be the same for using the PCIe 3.0 Protocol Test Card
- To capture trace, the Interposer probe can be placed into either one of the two Link3 connectors (under Exerciser or under the DUT)





Time: 4:50 - 5:20

System Configuration
Probes – Interposer, Flying Lead (solder down), & Midbus

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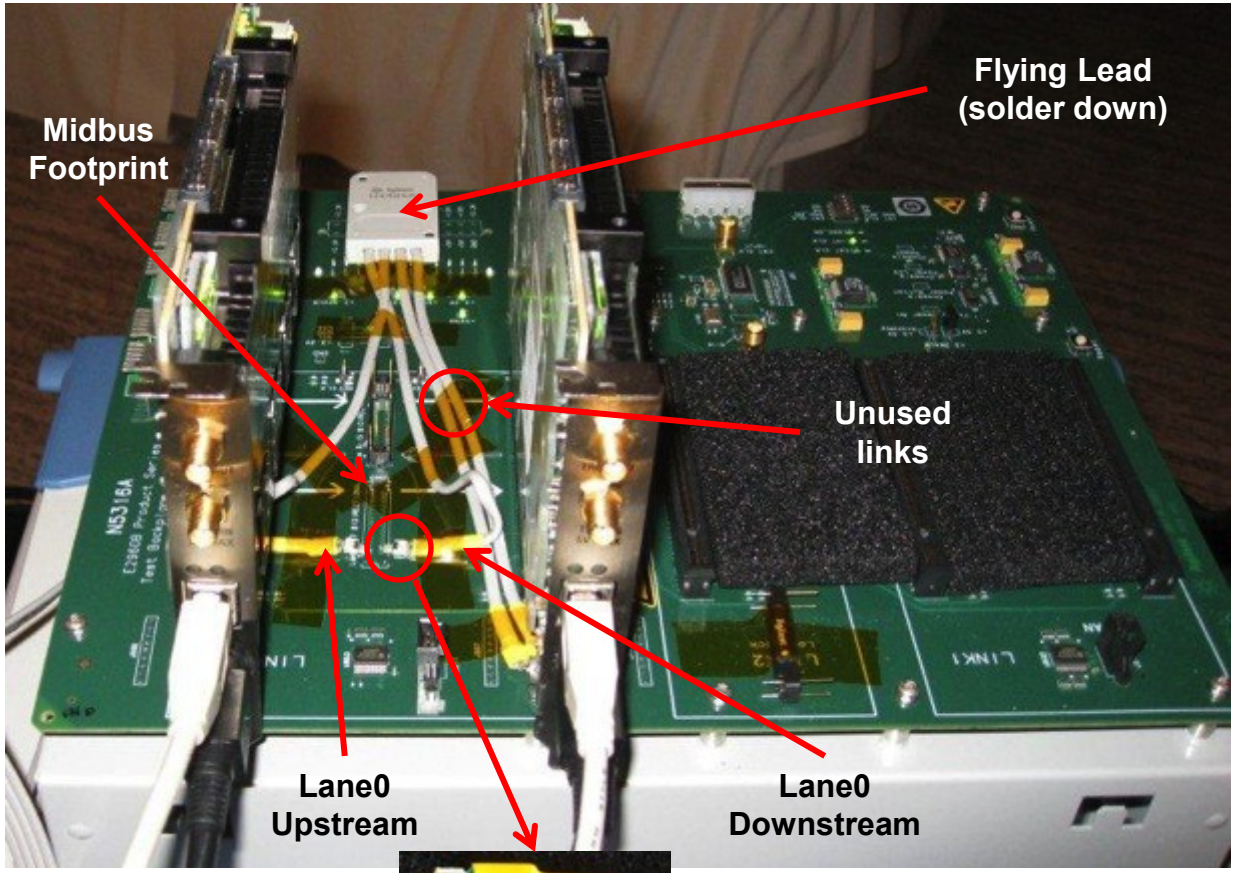
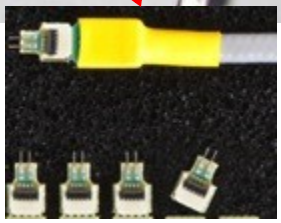
- The Interposer, Midbus, and Flying Lead probes all serve the same purpose; send upstream and downstream protocol traffic to the analyzer
- Ideally, all probes should have a large enough input impedance to be 'invisible' to both end-nodes of the channel under capture
- Any probe can be used in place of another provided the correct connection point exists
  - Interposers require a PCIe slot connector
  - Midbus requires a PCI-SIG spec'd footprint masked into the copper trace
  - A solder-down lead requires an end node Si pin differential pair or a test point differential pair



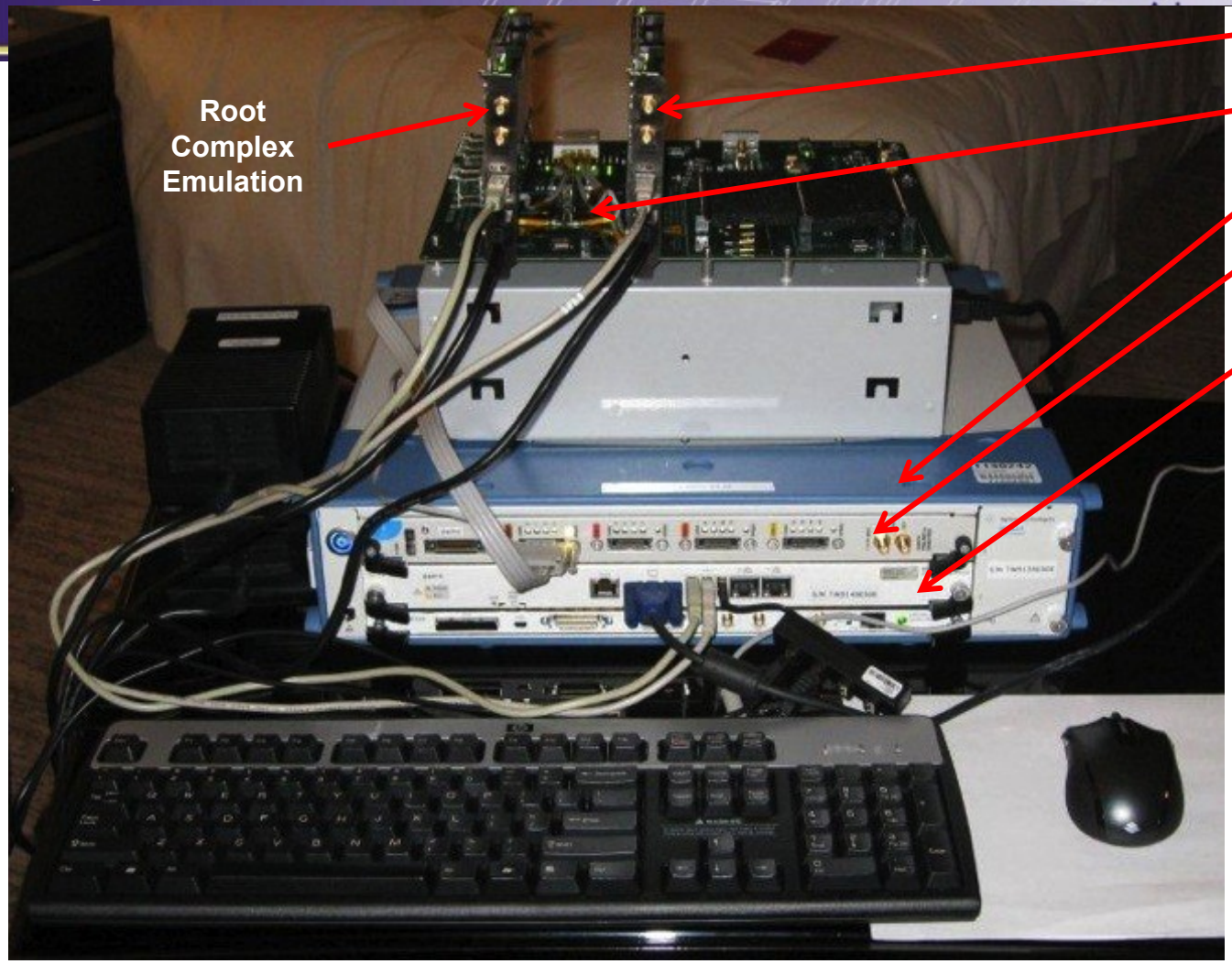


Flying Lead Zero Insertion Force (ZIF) Tip soldered to Lane0 of the upstream and downstream channel

Time: 4:50 - 5:20

System Configuration

Putting it all together …PCIe 3.0 Trace Capture Top to Bottom



- DUT Emulation
- Protocol trace capture using solder down probe
- PCIe AXIe Chassis
- PCIe 3.0 Protocol Analyzer
- Embedded Controller is the host for the Exerciser software and the Protocol Analyzer software

Time: 4:50 - 5:20

Open Discussion
Next Actions

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Open Discussion:

Next Actions:

- **Email response to reflector:** ***Would you attend a private reception at FMS if invited?***
- **Survey: Feedback on Meetings; Questions & Comments for Mtgs. No. 7-8**
- **Agenda & Topics**
  - **Meeting No. 5 - Big Picture; What's it all Mean**
    1. **How IOs Traverse the SW/HW Stack & Implications for PCIe** - Tom West, HyperIO
    2. **PCIe Standards: How they fit together** - Paul Wassenberg, Marvell
    3. **PCIe, SCSI Express, and a world beyond disk drives; What happens when you get new native flash capabilities** - Gary Orenstein, Fusion-io
  - **Meeting No. 6 - Deployment Strategies / Market Development**
    1. **PCIe as Persistent Storage** - Walter Hubis, Fusion-io
    2. **OPEN** - ***contact chair if you are interested to present***

Time: 5:20 - 5:30

Supplemental Slides